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MS-7A82

ATX:243*183
Ver: 1.0

Intel -SkyLake-S plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase
GT POWER PAK *2 Phase

System Chipset:

PCH-H :H110

Onboard Chip:

HD Audio Codec: ALC887
SIO: NCT6793D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

PWM:

VCORE - RT3606BC
DDR - RT8231AGQW
DDR - VPP25 - MP21473
PCH(1.0V) - RT8125E
VCCSA - RT8125E
VCCIO - NB681(Converter)

Main Memory:

DDR4 * 2 (Dual Channel)

LDO:


VCCSTPLL - GS7133

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133
3VDSW:GS7116S

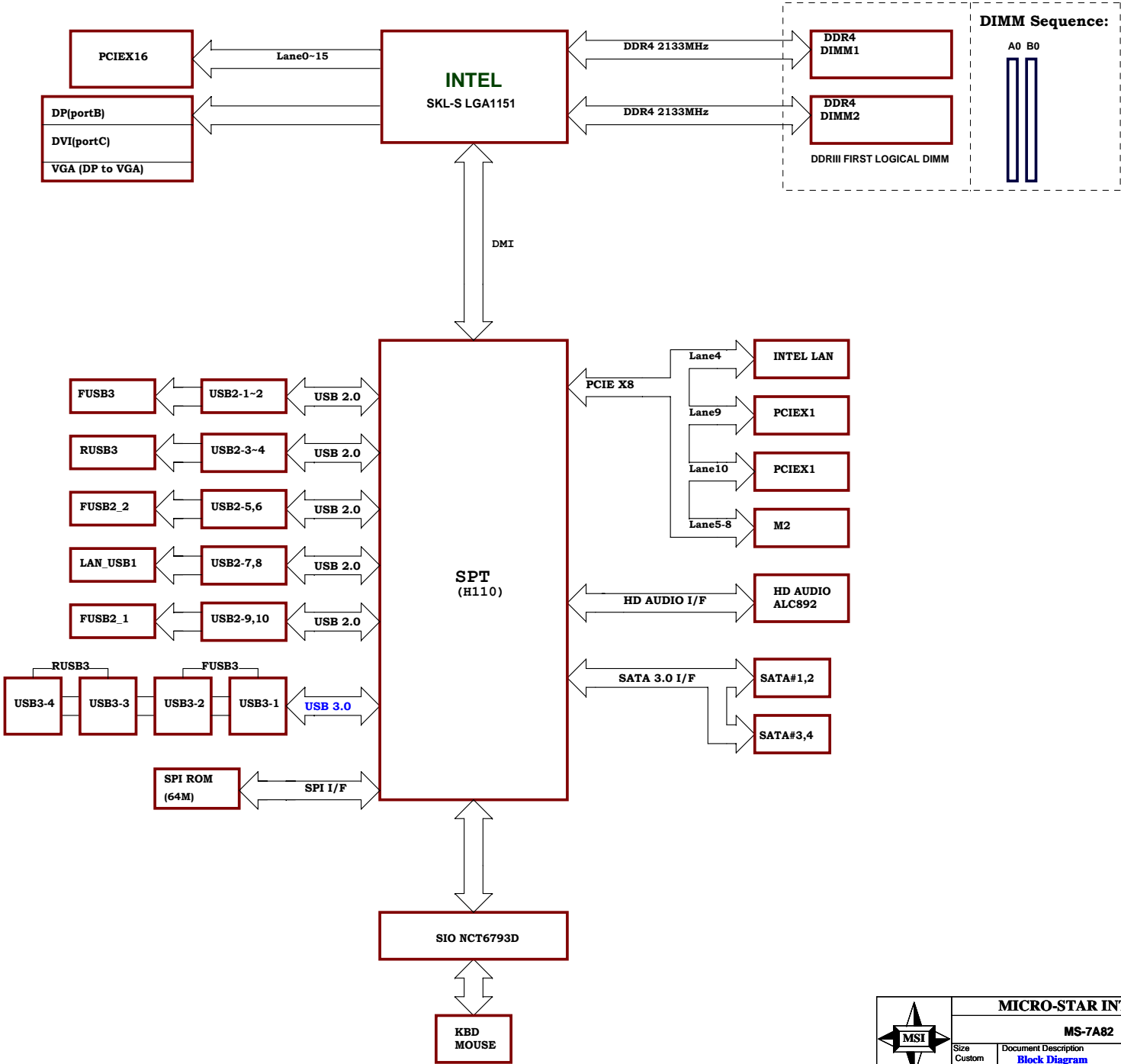
Expansion Slots:

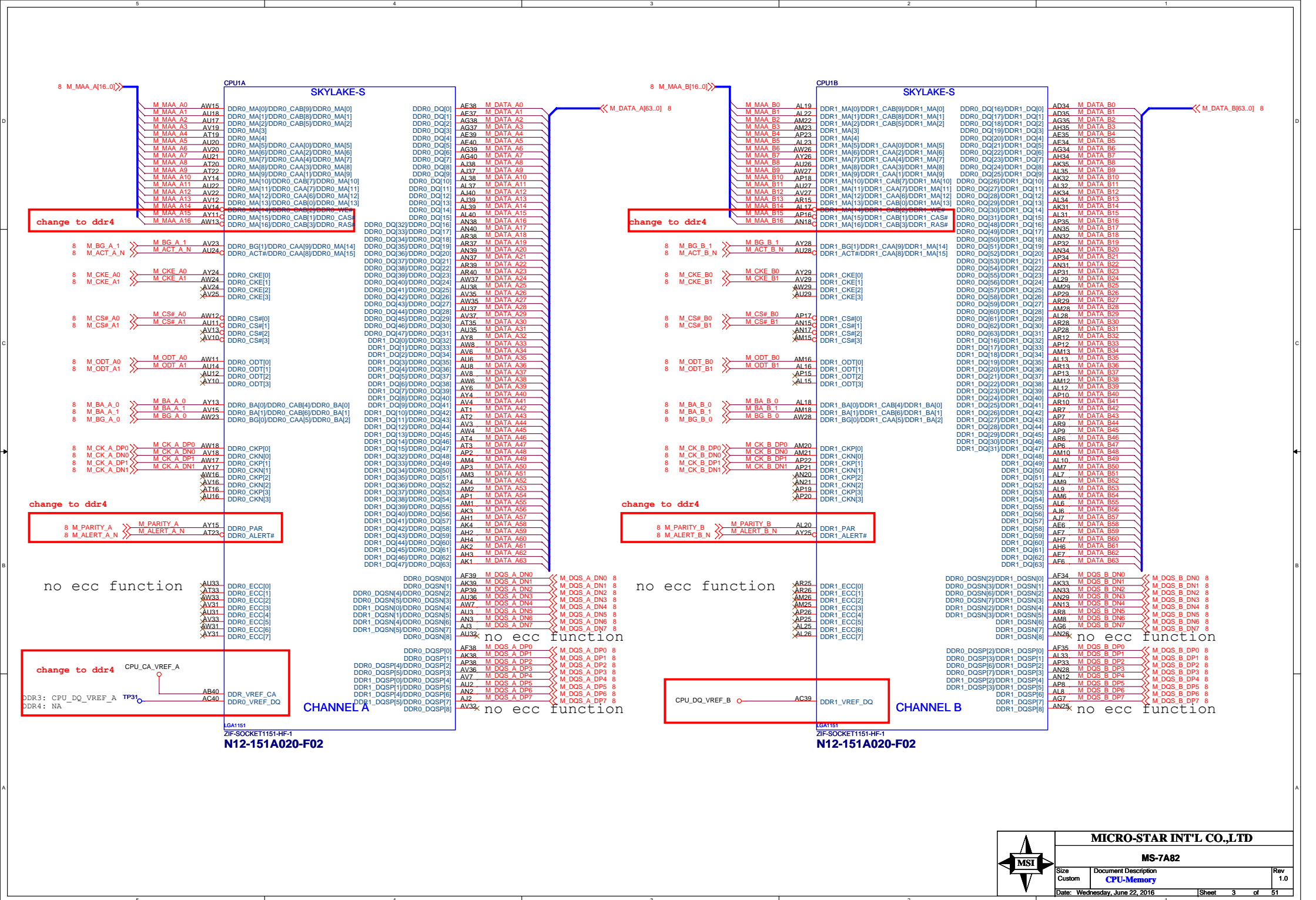
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2



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MS-7A82		
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MS-7A48 Block Diagram





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MS-7A82

Size

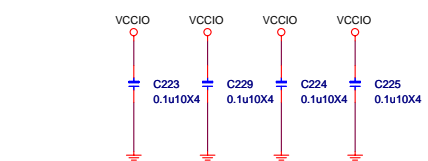
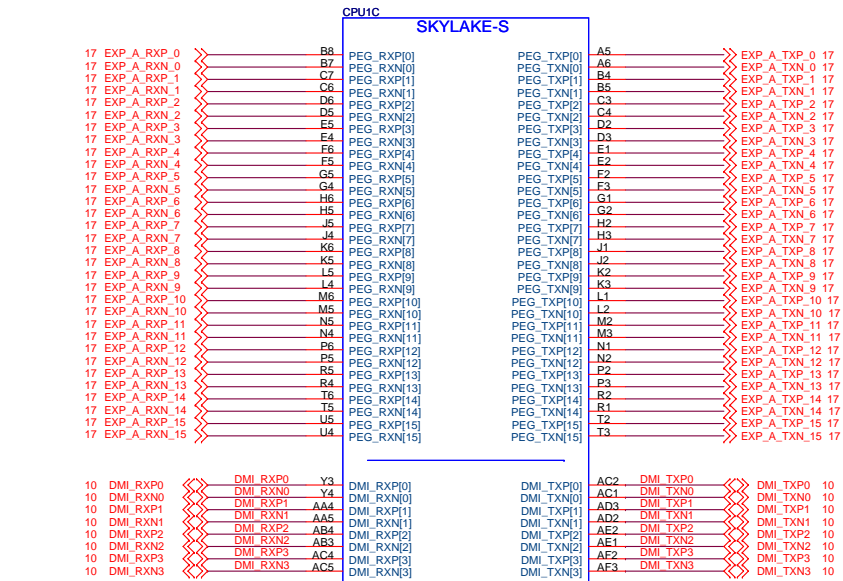
Document Description

Rev	
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Custom

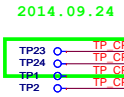
CPU-Memory

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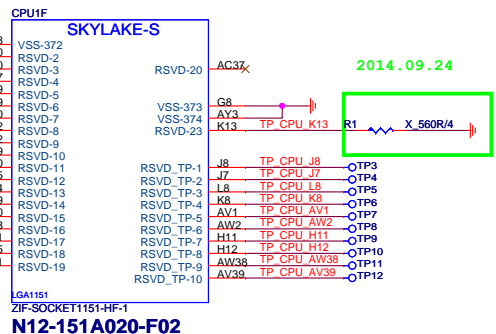
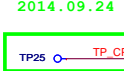


For DMI reference VCCIO USE please close to DMI via side

CRB 1.0 update
Add TP23,TP24
For Test

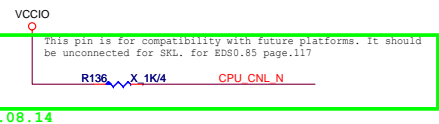
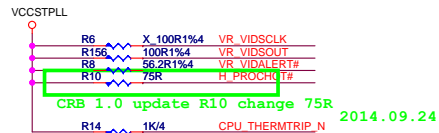
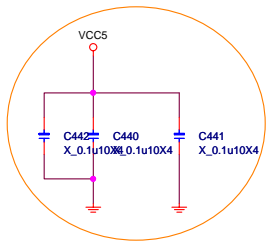


CRB 1.0 update
TP25
For Test



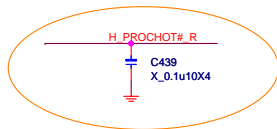
2014.09.24

CRB 1.0 update
CRB unstuff
PCB come back remove

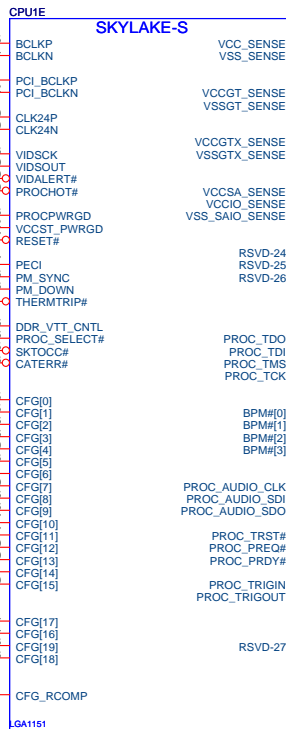


CFG Strap

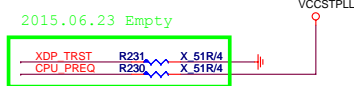
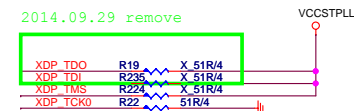
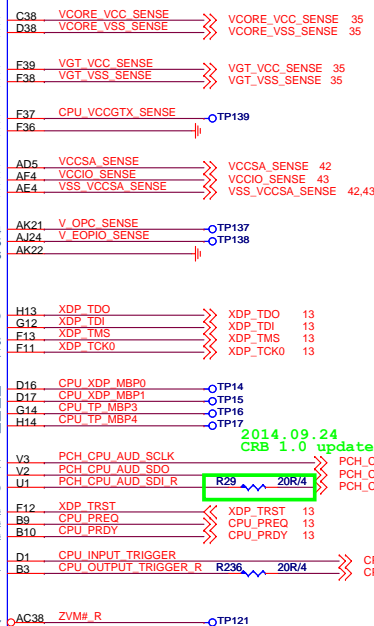
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CPGSEL[0]
6	DISABLE	ENABLE	PEG0CPGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD



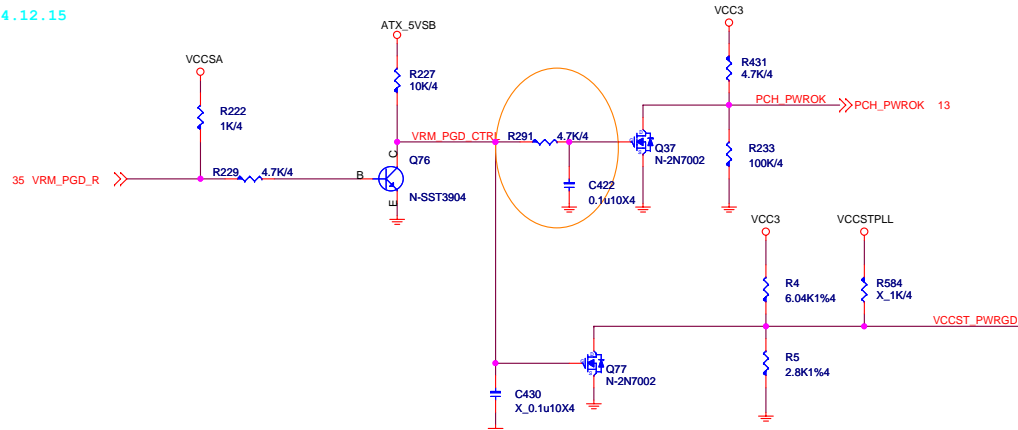
CRB 1.0 update RSVD
Detail refer CRB 1.0
2014.09.24



MSI
ZIF-SOCKET1151-HF-1
N12-151A020-F02

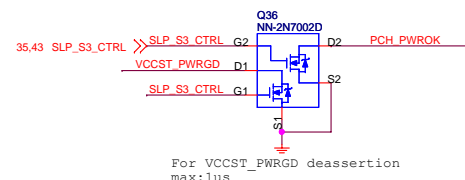


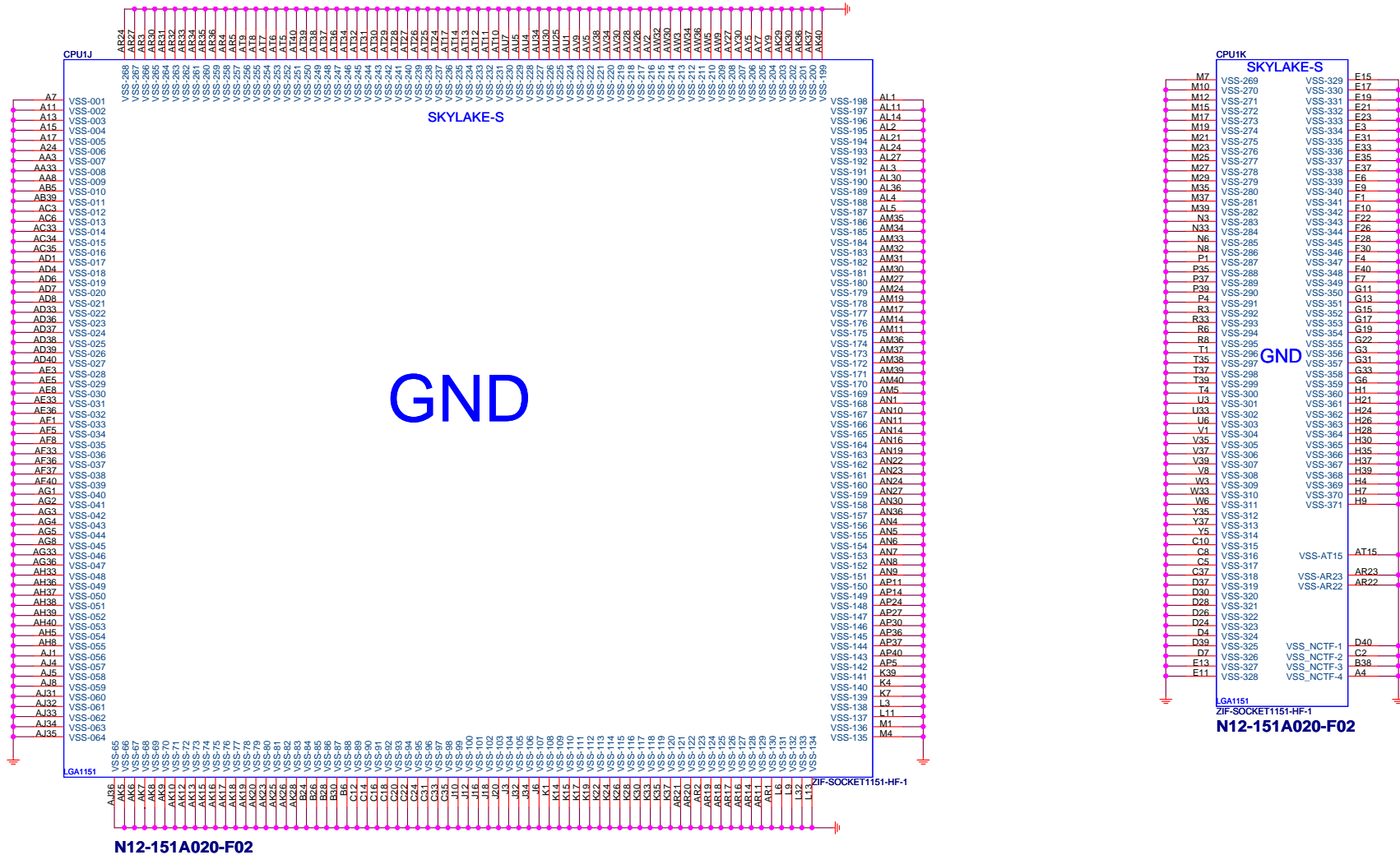
modify 2014.12.15

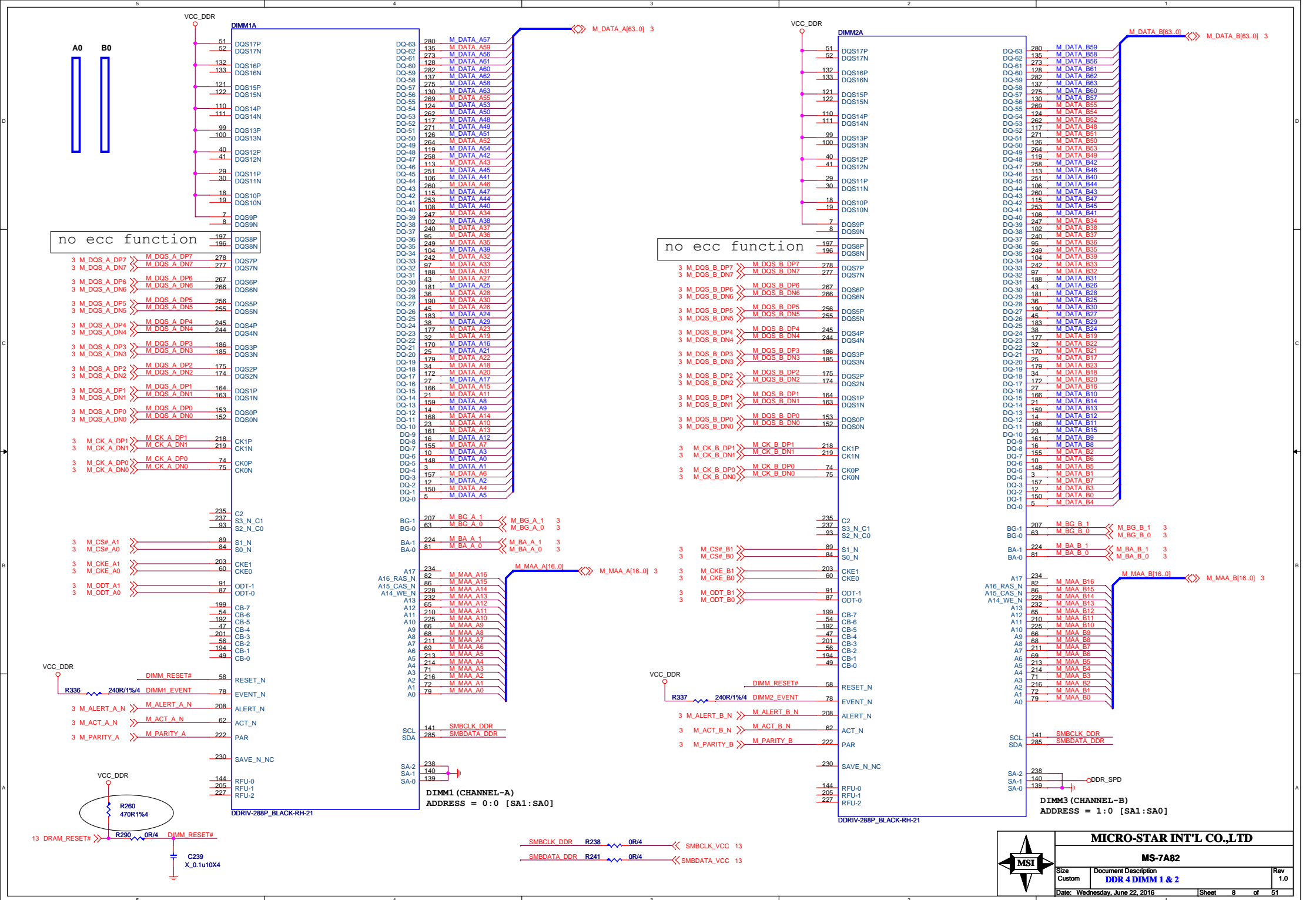


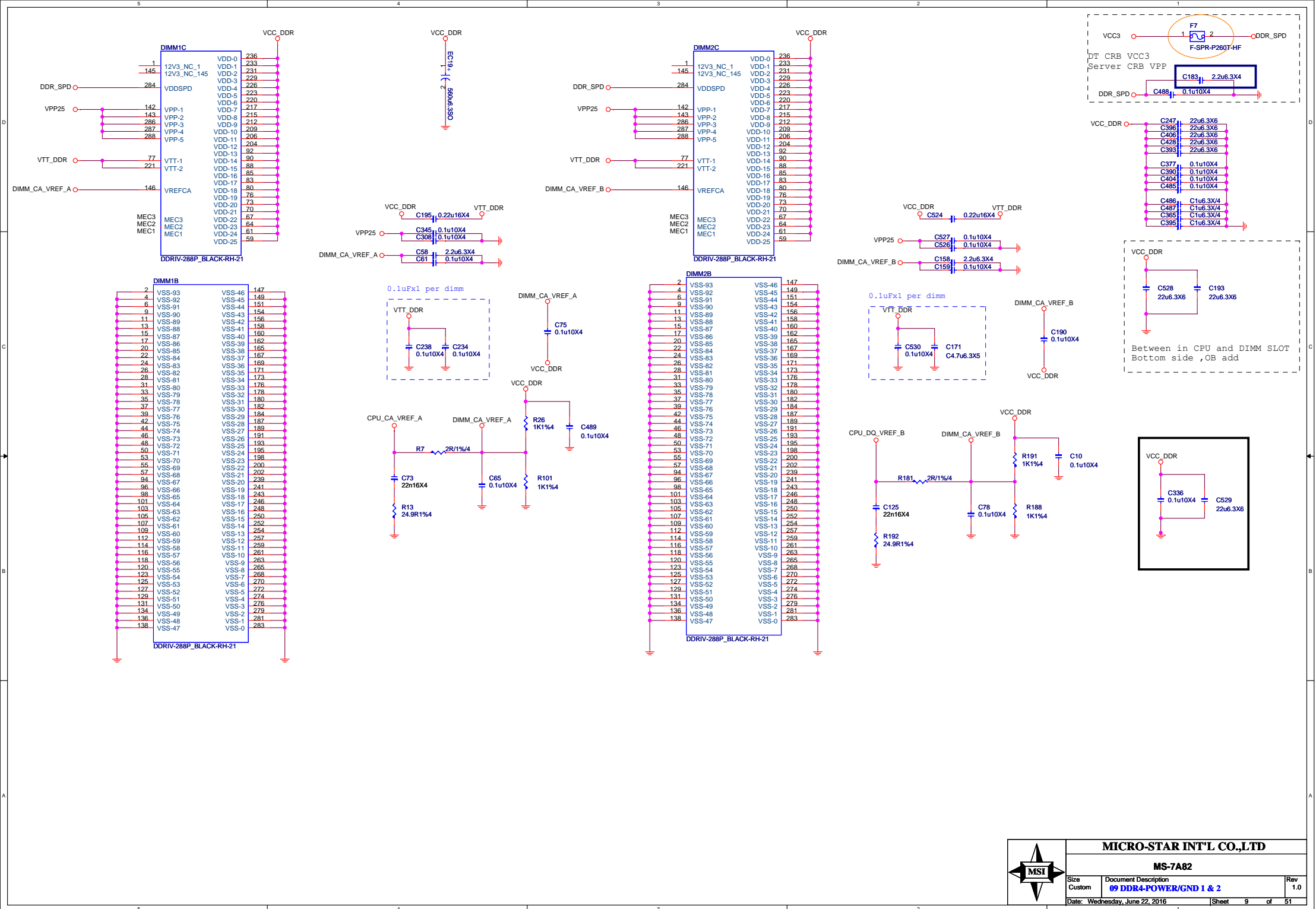
modify 2014.09.19

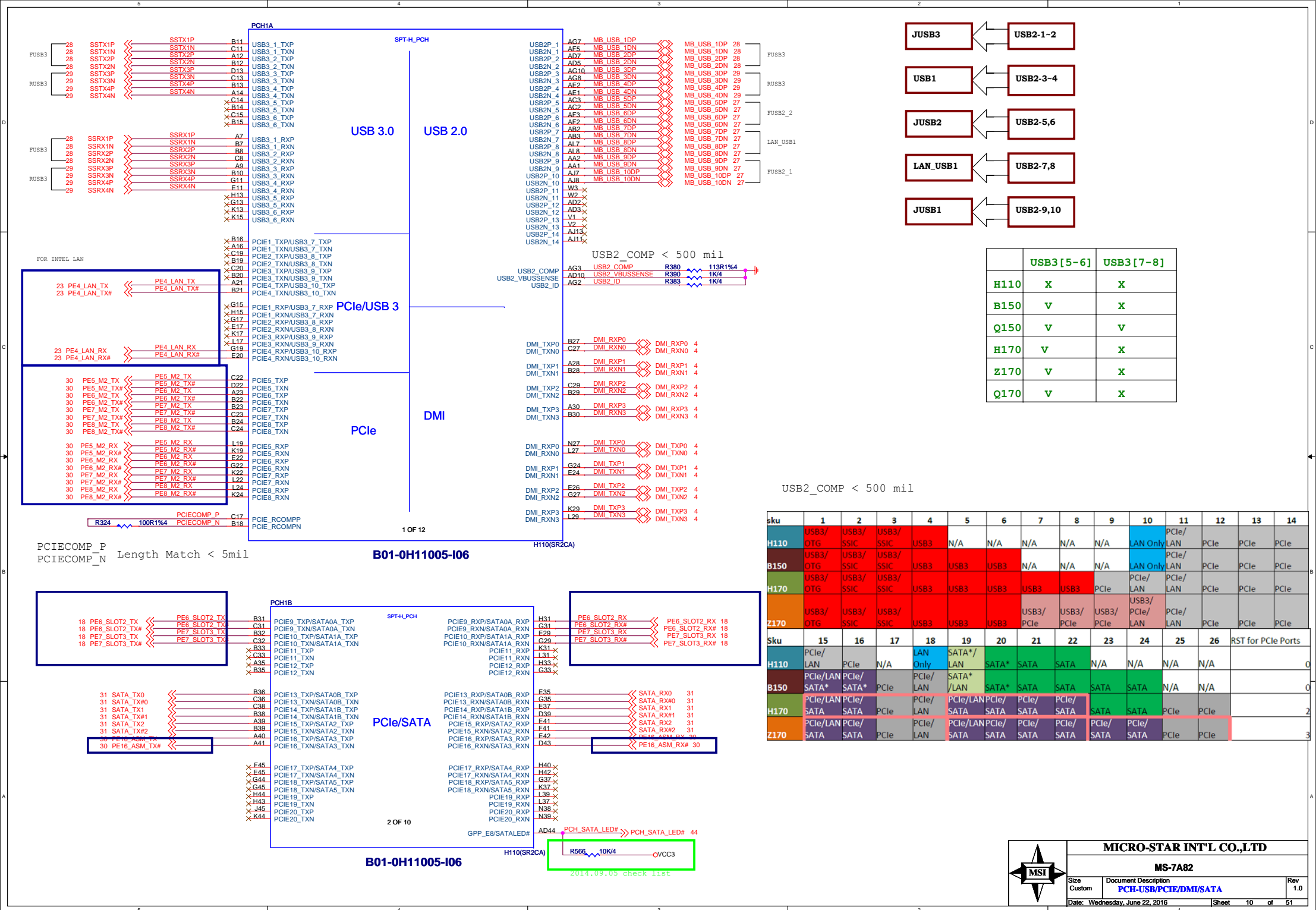
POWER DOWN

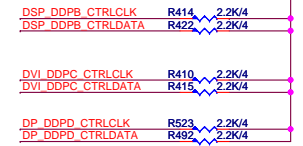
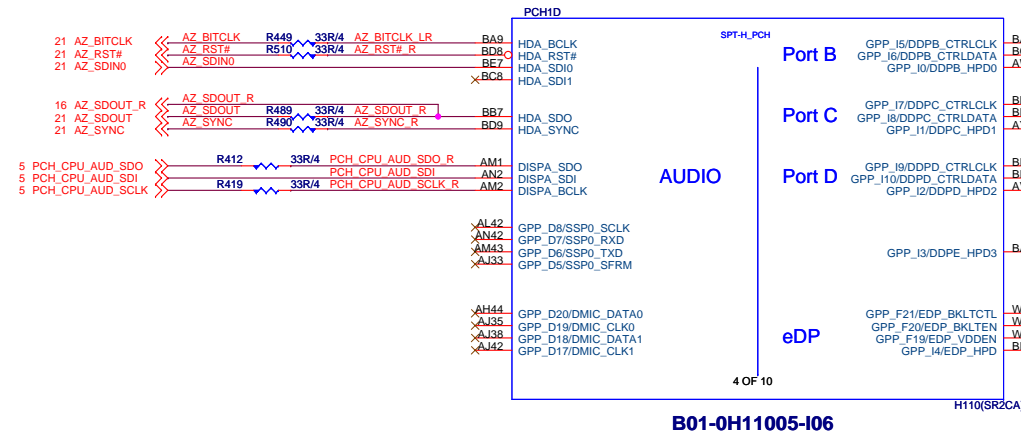
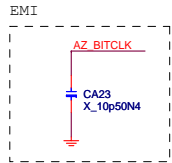




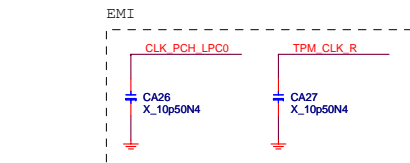




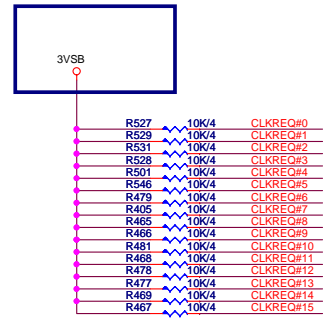
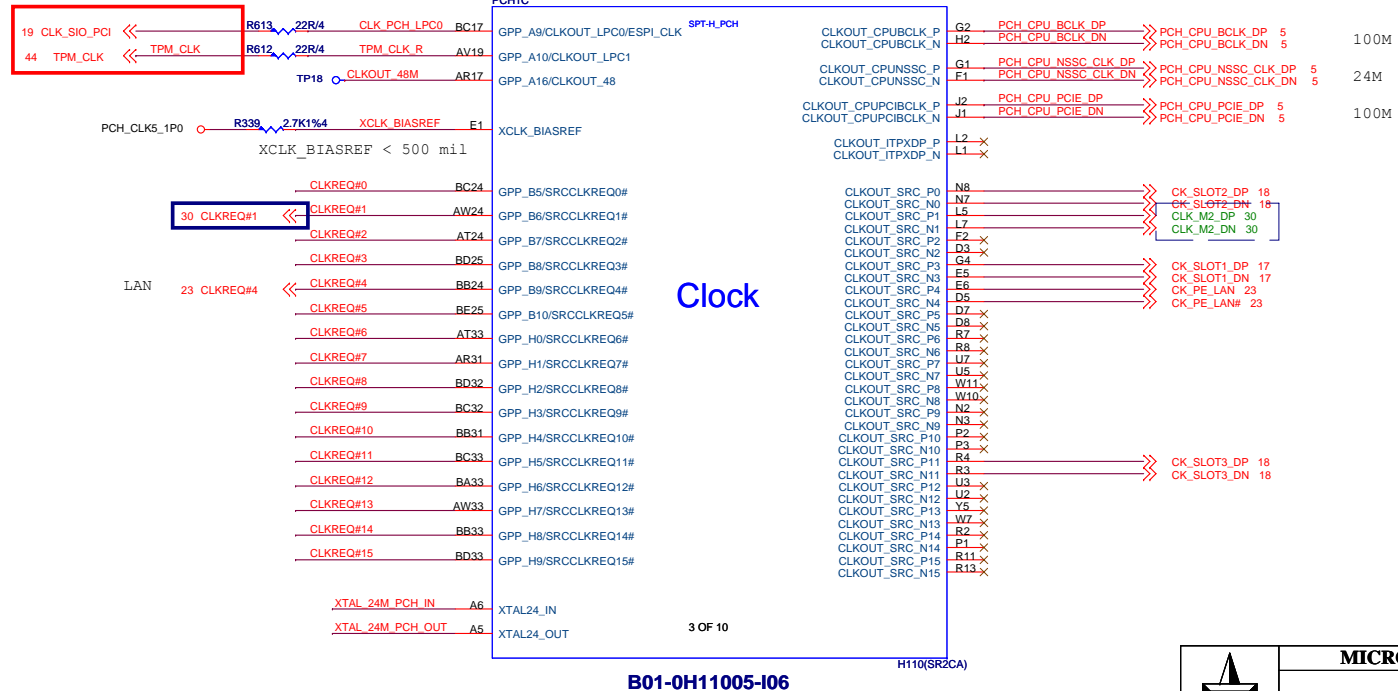




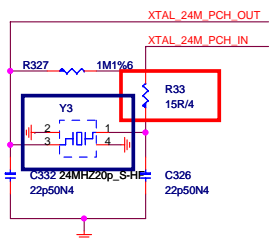
DDI interface Disable
no connect
Port B HDMI
Port C DVI, HDMI2.0 OR Others
Port D DisplayPort



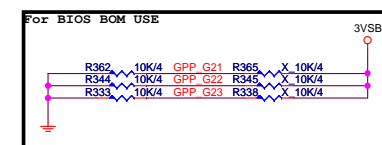
2015.12.24 remove CLOCK BUFFER



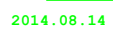
Connect to SLOF Pin B12
for support L1 PM Substates
MS also can disable this function.



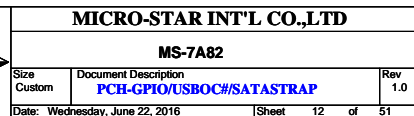
MICRO-STAR INT'L CO.,LTD			
MS-7A82			
Size	Document Description	Rev	
Custom	PCH-Audio/Display/Clock	1.0	
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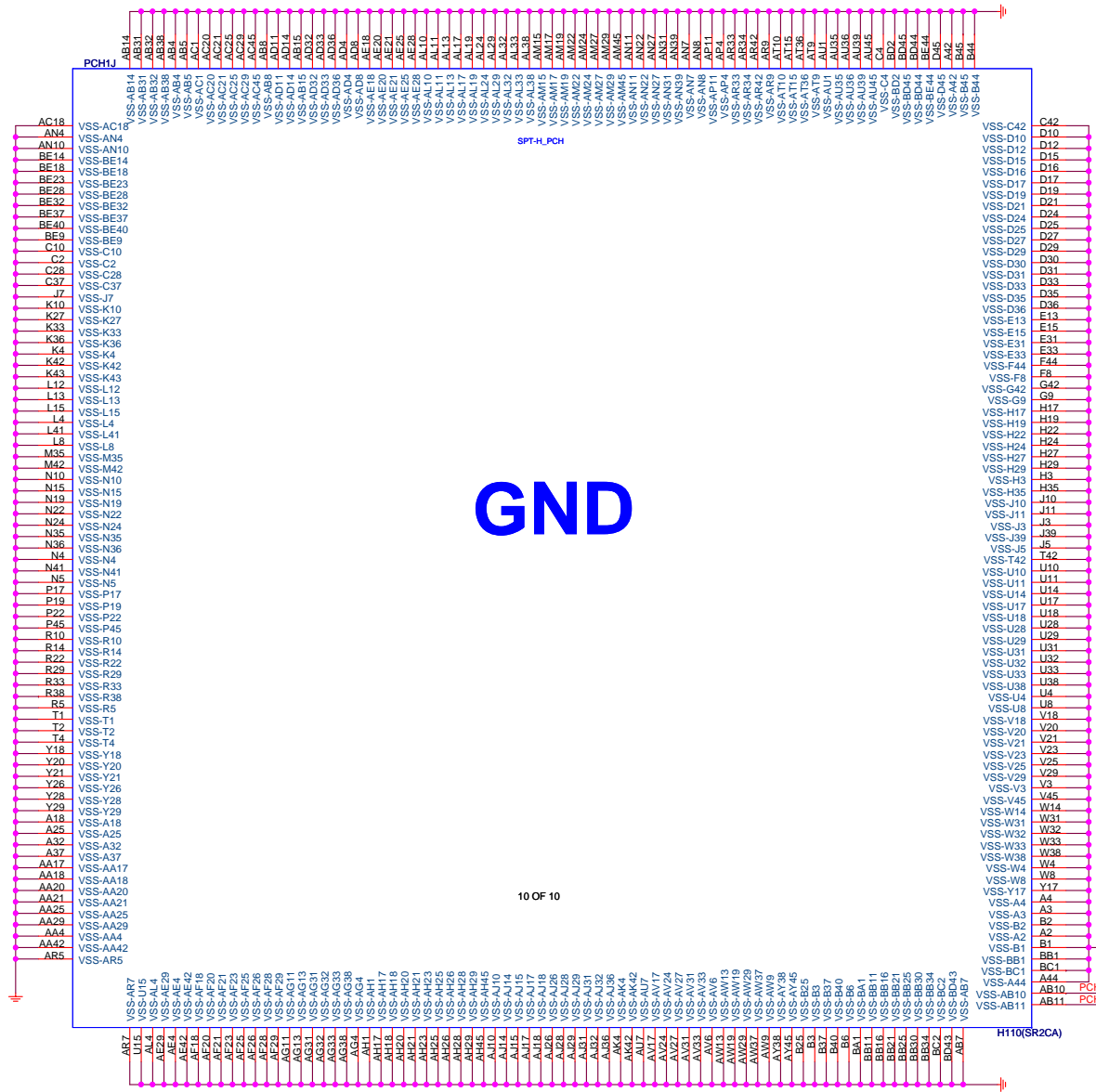


When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



If an AMT capable Intel WLAN device is not implemented then this signal can be left as NO CONNECT (NC).

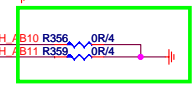




GND

10 OF 10

B01-0H11005-106

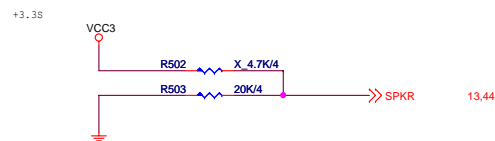


CRB 1.0 update
R356,R359 stuff
2014.09.24



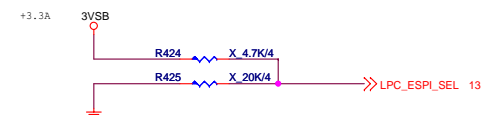
MICRO-STAR INT'L CO.,LTD		
MS-7A82		
Size	Document Description	Rev
Custom	PCH-GND	1.0
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

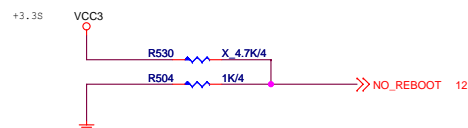
LPC eSPI Mode



```
0 : LPC
1 : eSPI
```

Internal pull-down 20K is disabled after RSMRST

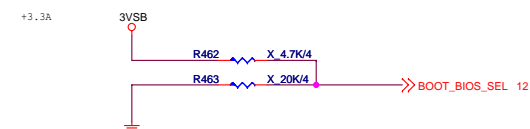
No Reboot



```
0 : DISABLE (Default)
1 : ENABLE
```

Internal pull-down 20K is disabled after PLTRST#

Boot BIOS



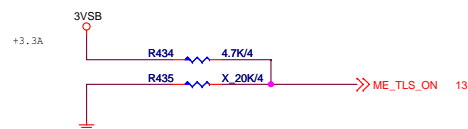
```

0 : SPI
1 : LPC

```

Internal pull-down 20K is disabled after PLTRST

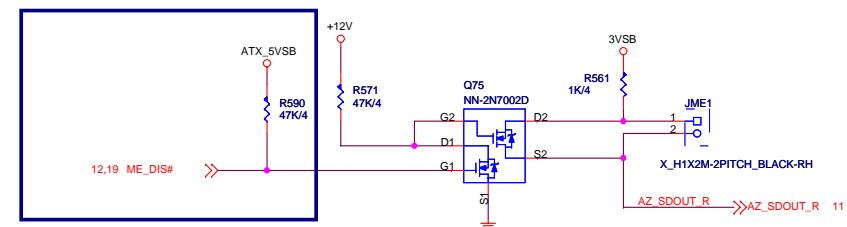
AMT and SBA with confidentiality



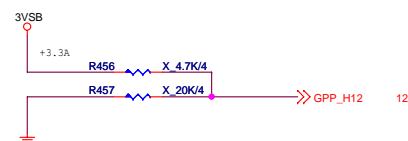
```
0 : DISABLE
1 : ENABLE (Default)
```

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



```
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING
```

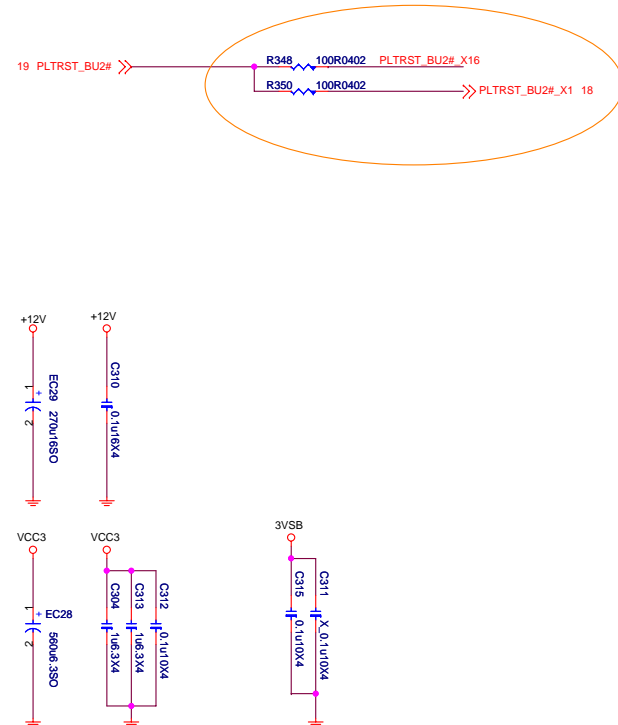
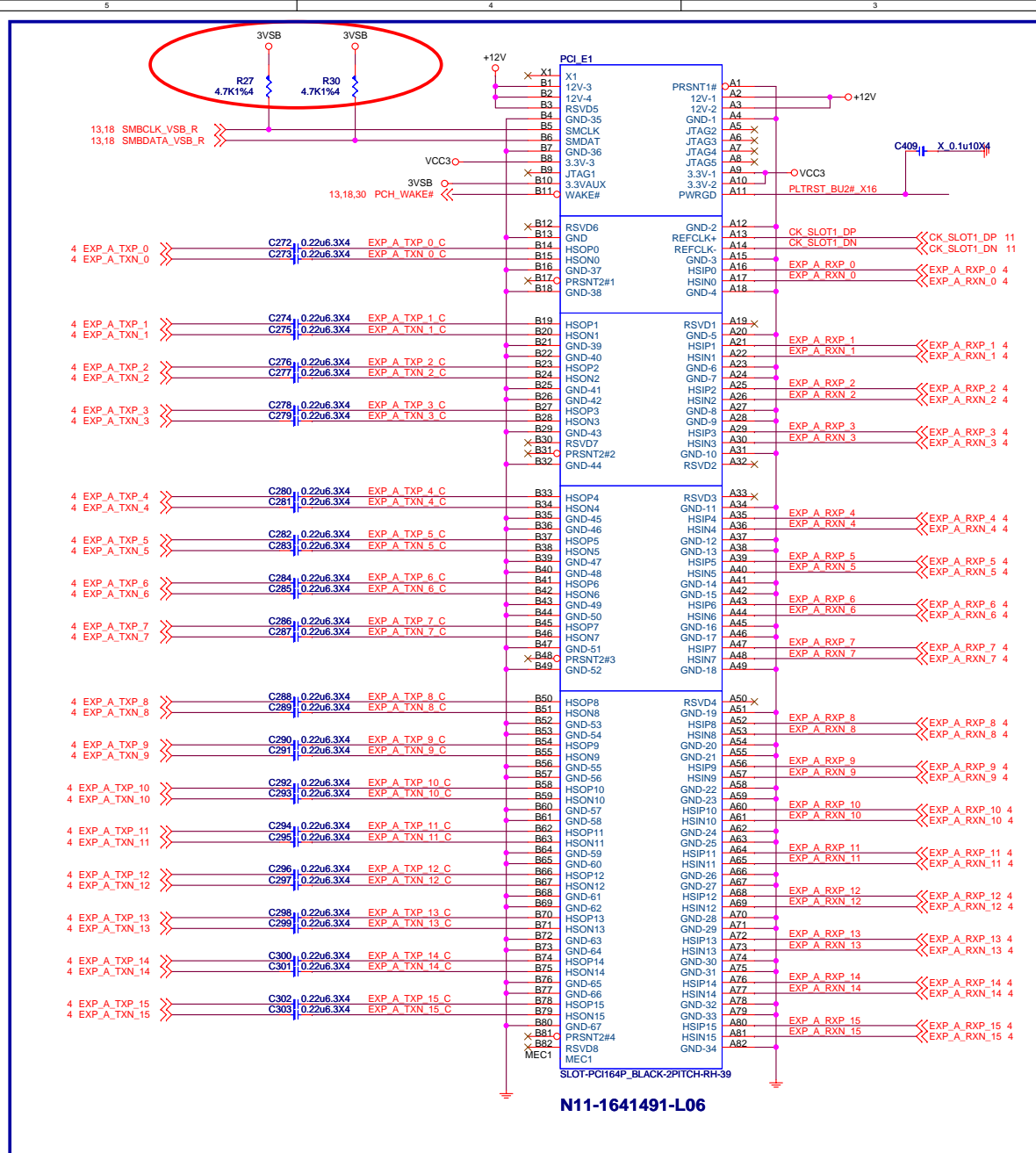
Internal pull-down 20K is disabled after RSMRST

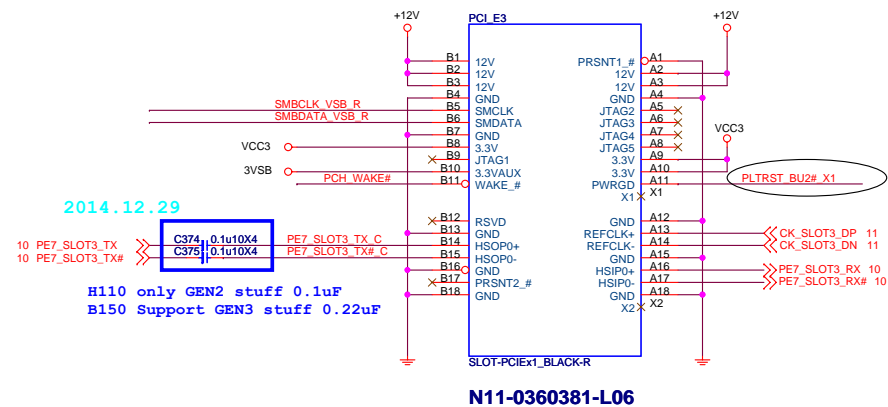
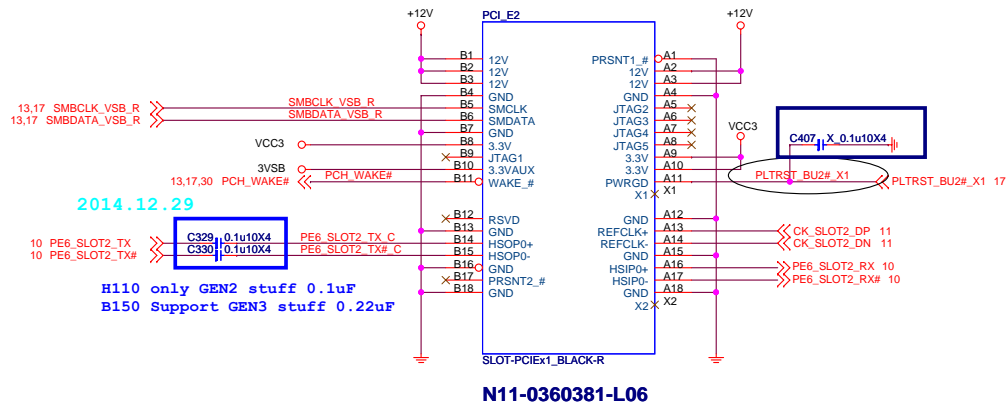


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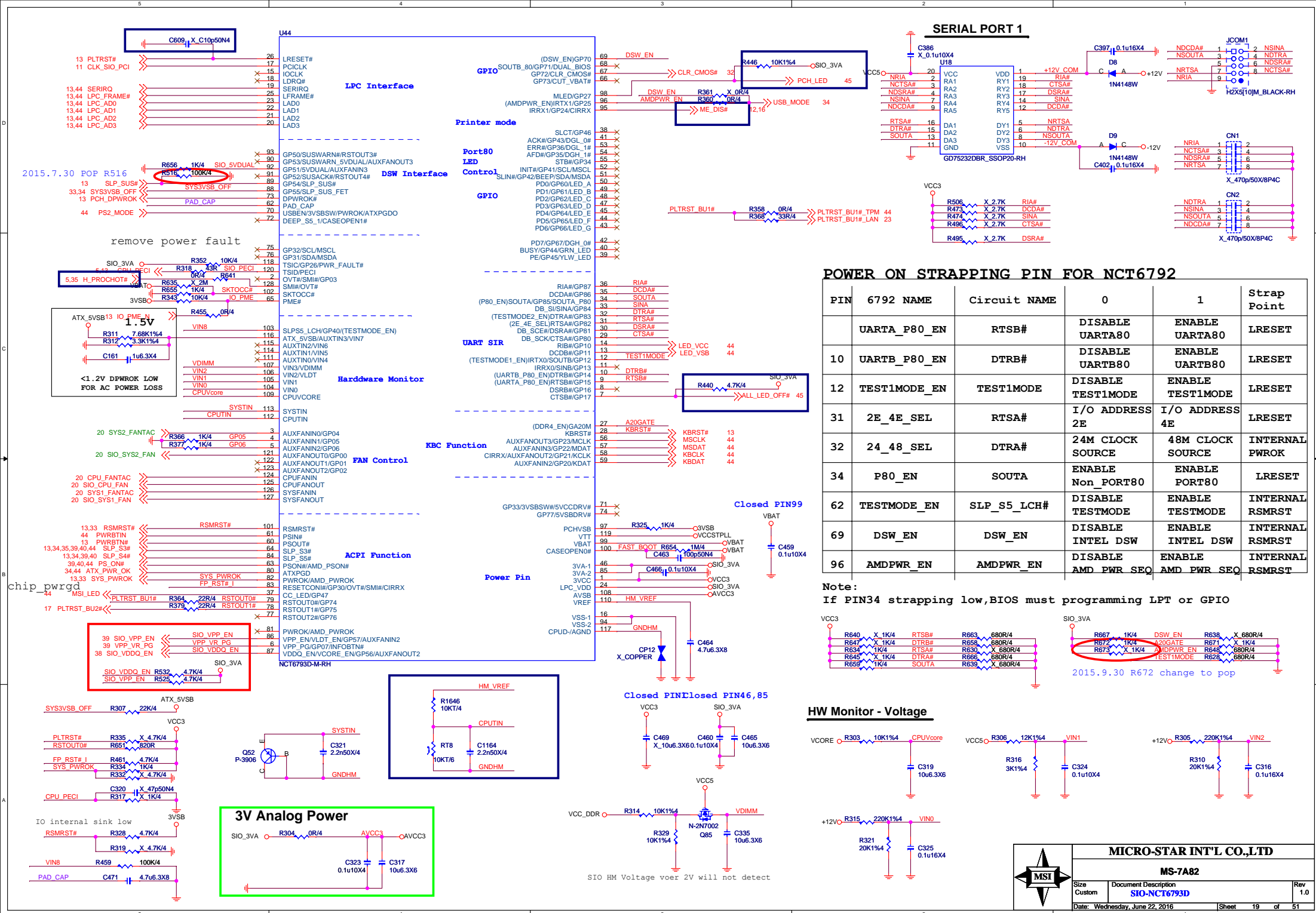




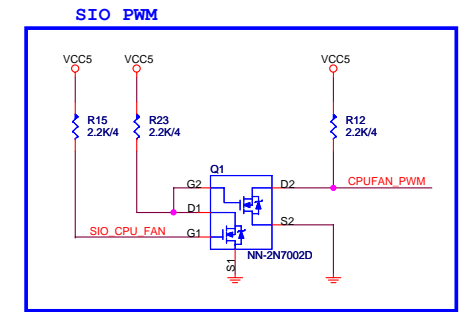
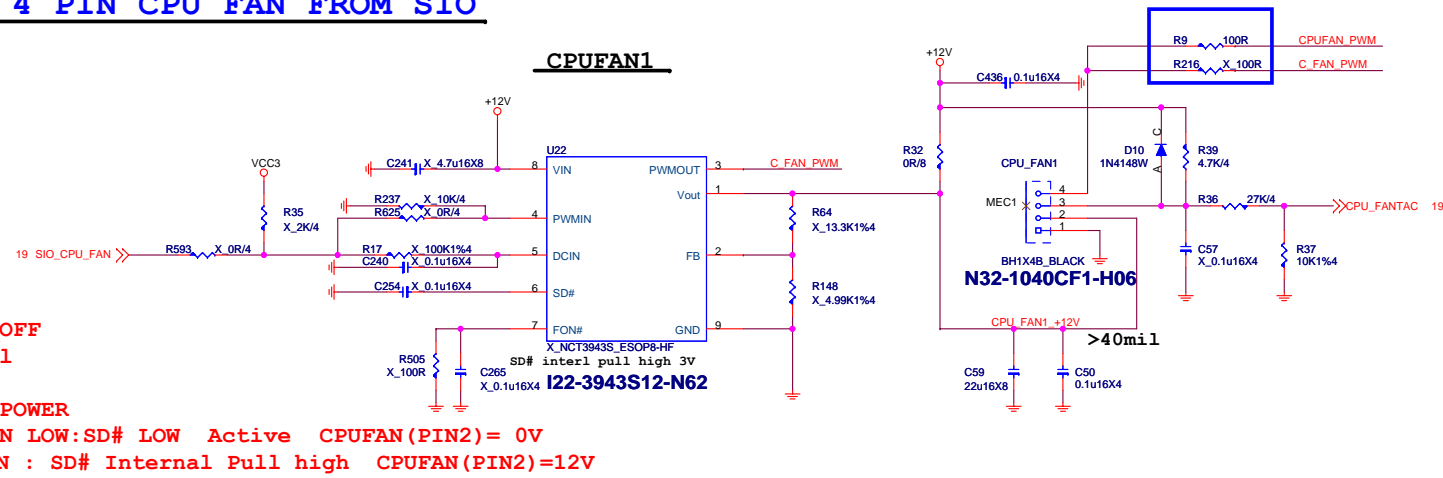
MICRO-STAR INT'L CO.,LTD

MS-7A82

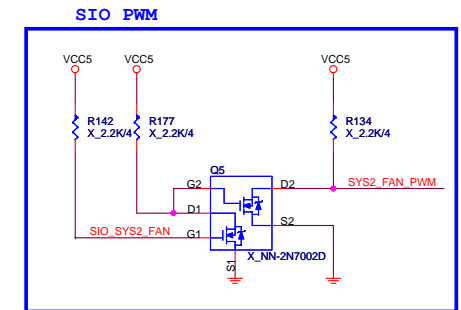
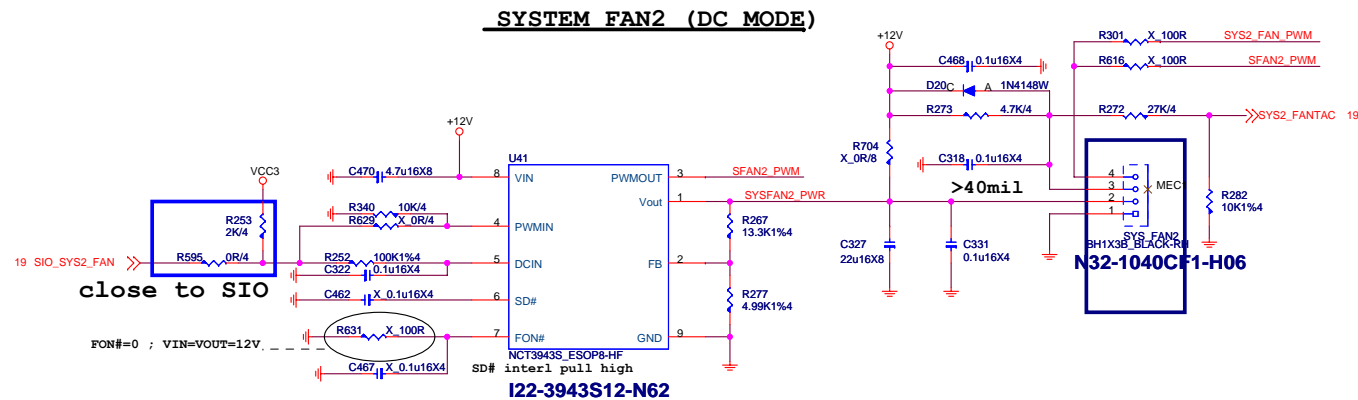
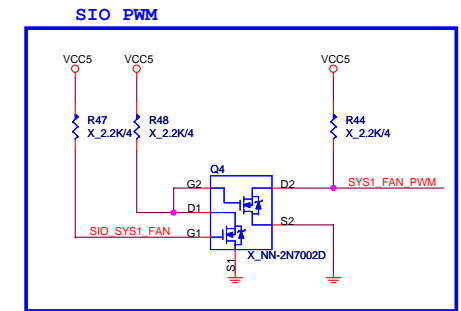
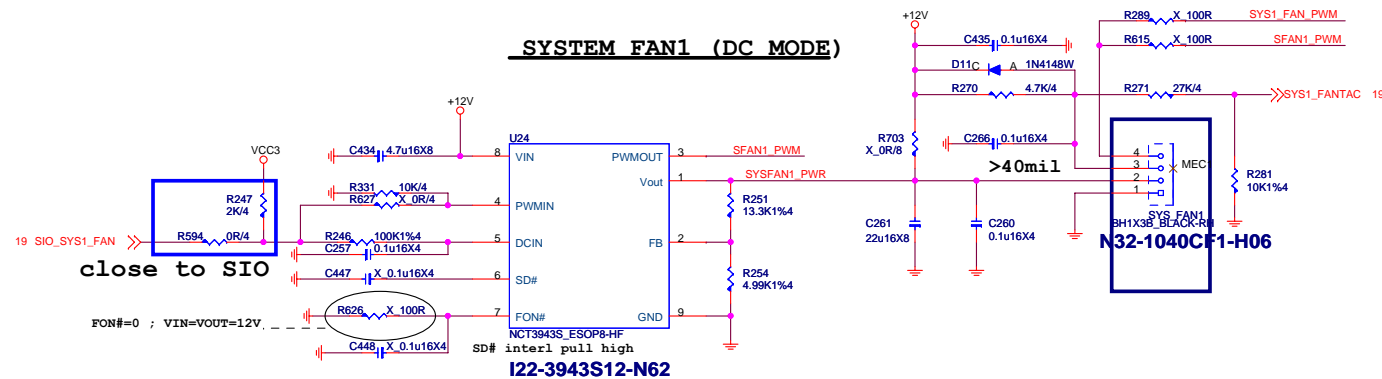
Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	1.0
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Type G : 4 PIN CPU FAN FROM SIO



Type H : 4 PIN SYS FAN FROM SIO

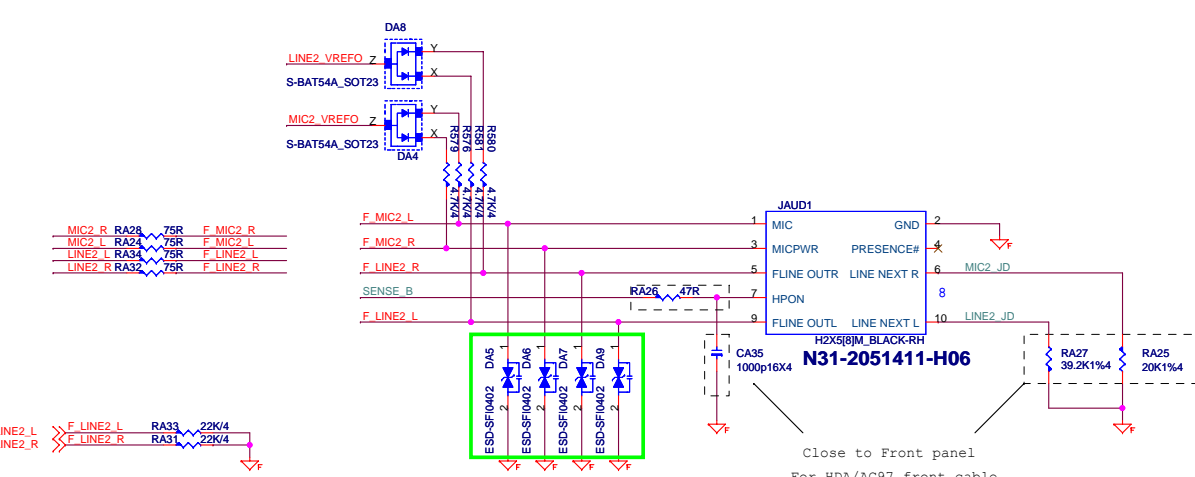
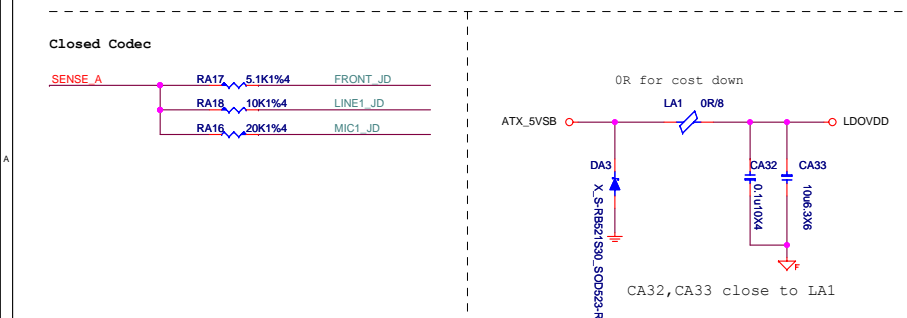
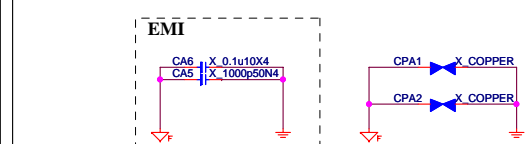
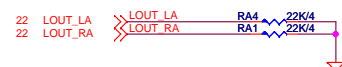
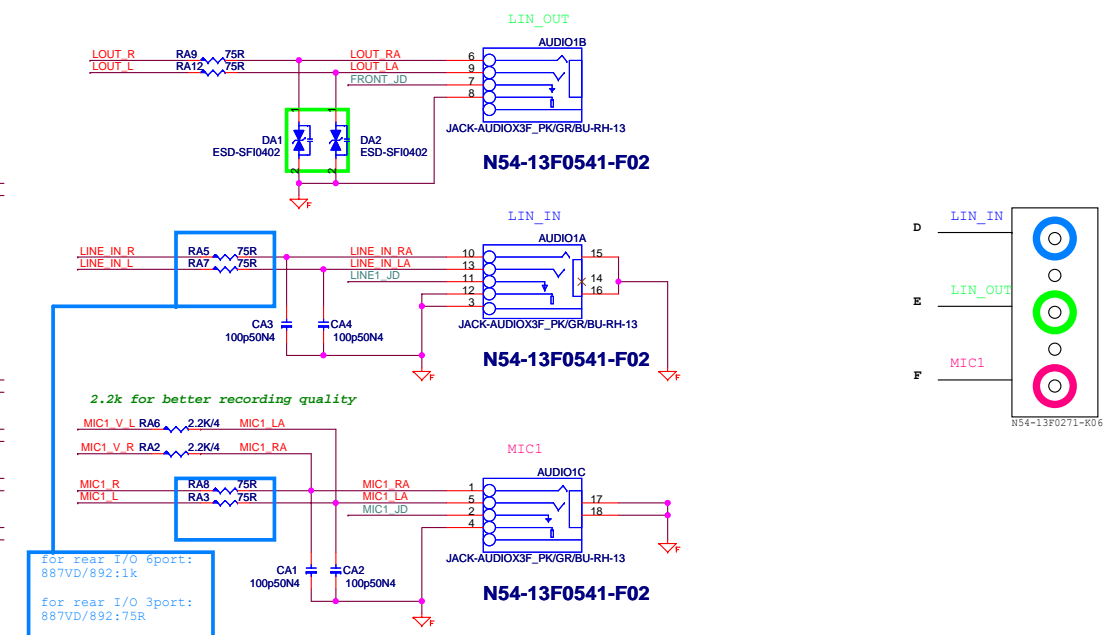
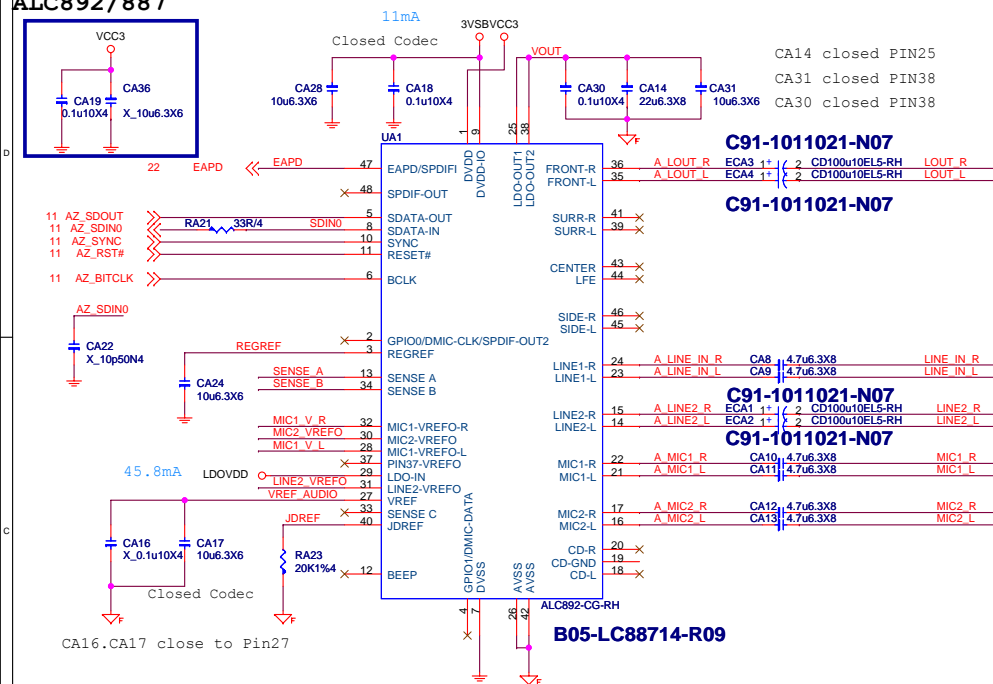


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description FAN CONTROLLER	Rev 1.0
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ALC892/887



Varistor --> cap for cost down

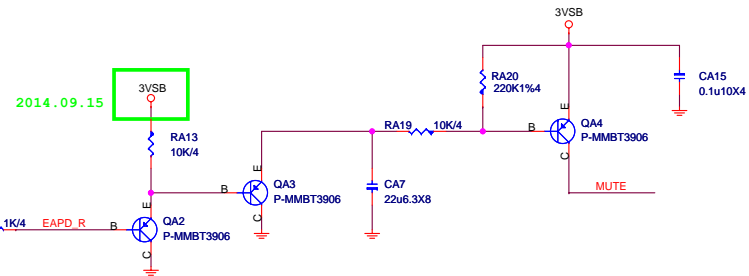
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack



MICRO-STAR INT'L CO.,LTD			
MS-7A82			
Size Custom	Document Description AUDIO - ALC892/887		Rev 1.0
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Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

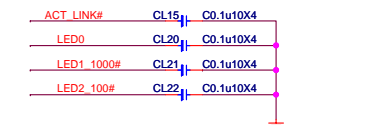
Analog



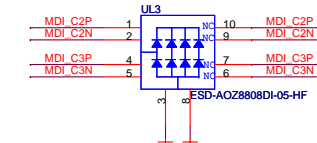
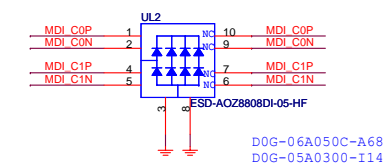
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

For EMI



UL2&UL3 close to connector



Do not pair MDIO and MDI1 on the same TVSdevice
(avoid LAN POE connecting issue).
Otherpairing combination is ok.

The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRO<n> buffer.

ATX_5VSB

3VDSW

RL20 47K

SLP_LAN

QL1

CL18 X_C1u6.3X4

P-006P03LOG_SOT89-3-RH

+3.3V LAN

+3.3V LAN

I218:132mA

I219:542mW

ALDPS

13 SLP_LAN#

RL22 20K1%4

CL19 C1u6.3X4

QL2 2N7002

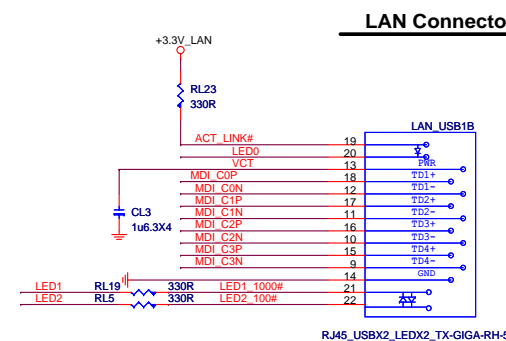
CL16 C22u6.3X8

CL17 C0.1u10X4

RL21 10K

Note: These caps closed to PHY

Note: These caps closed to PHY



RJ45_USBX2_LEDX2_TX-GIGA-RH-5

N58-22F0731-F02



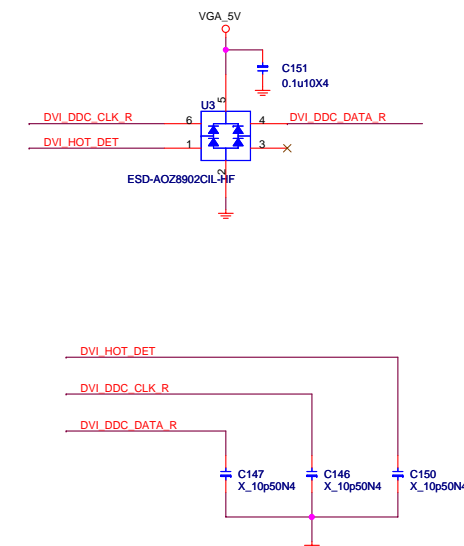
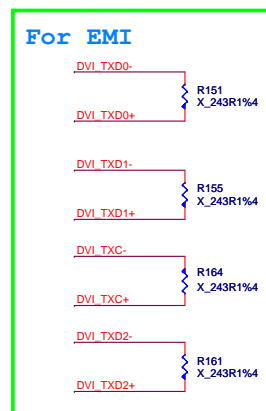
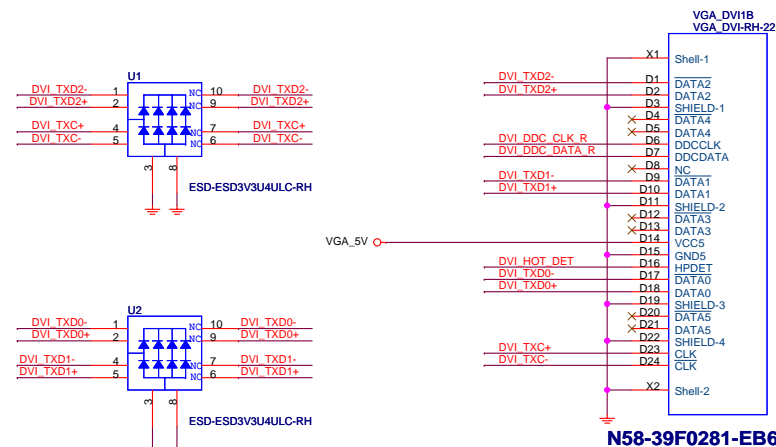
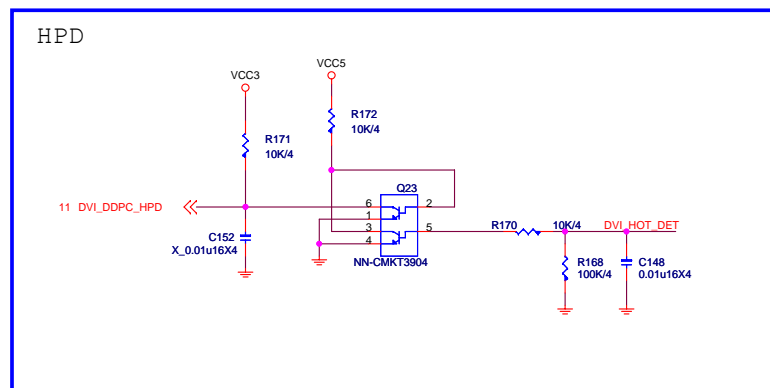
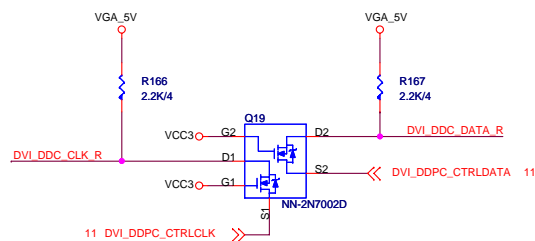
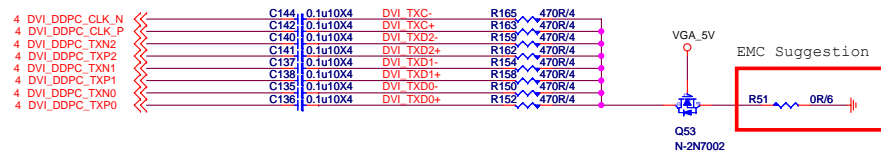
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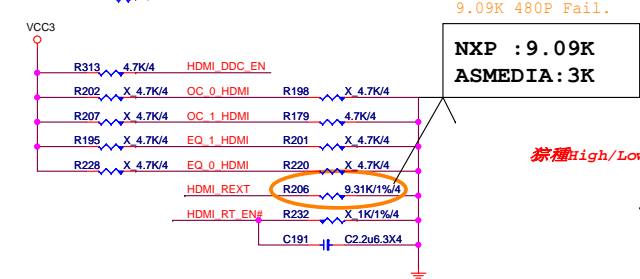
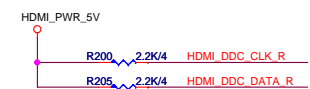
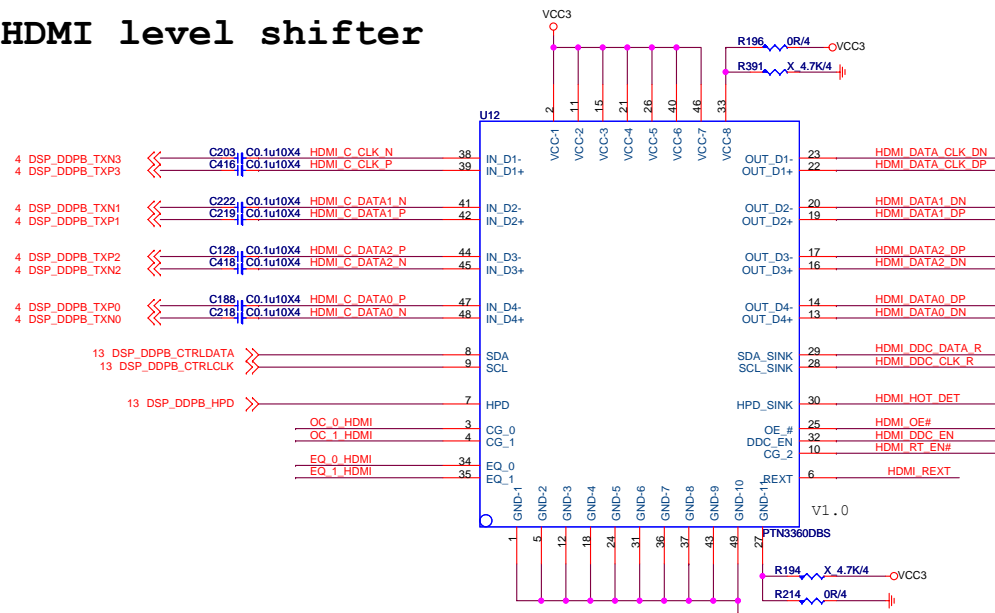
Size Custom	Document Description LAN - RTL8111H	Rev 1.0
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DVI level shifter

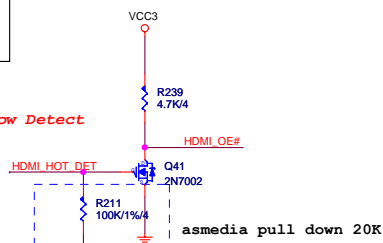
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI level shifter



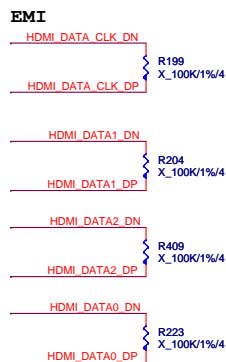
禁種High/Low Detect



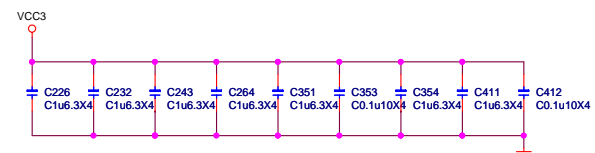
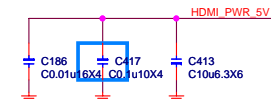
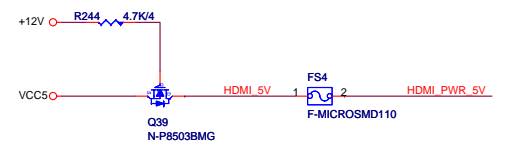
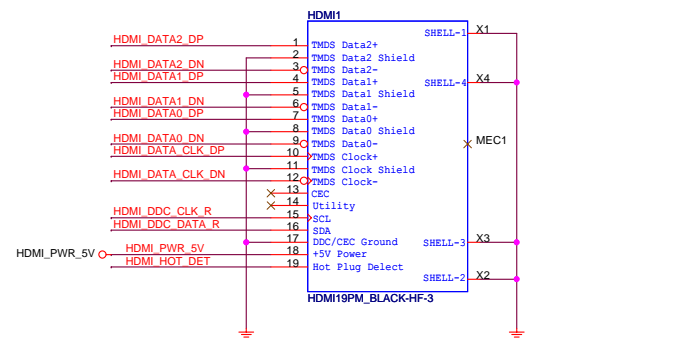
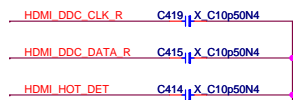
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0	generation.	note
00	8 dB	internal pull-up at ~500K ohm.
01	4 dB	internal pull-down at ~500K ohm.
10	12 dB	internal pull-down at ~200K ohm; 5V tolerant, internal pull-down at ~500K ohm.
11	0 dB	analog current



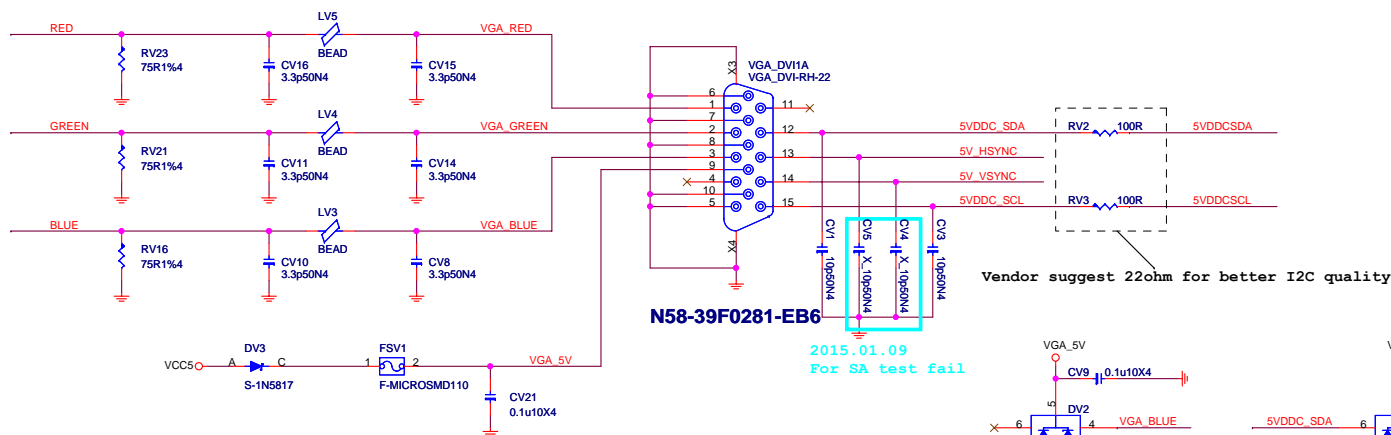
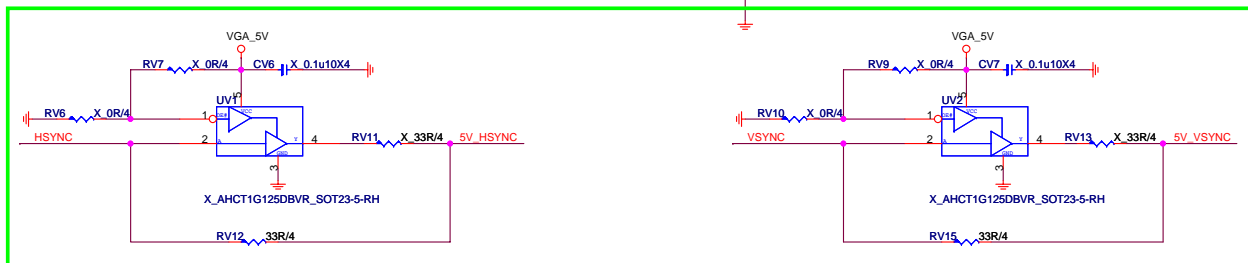
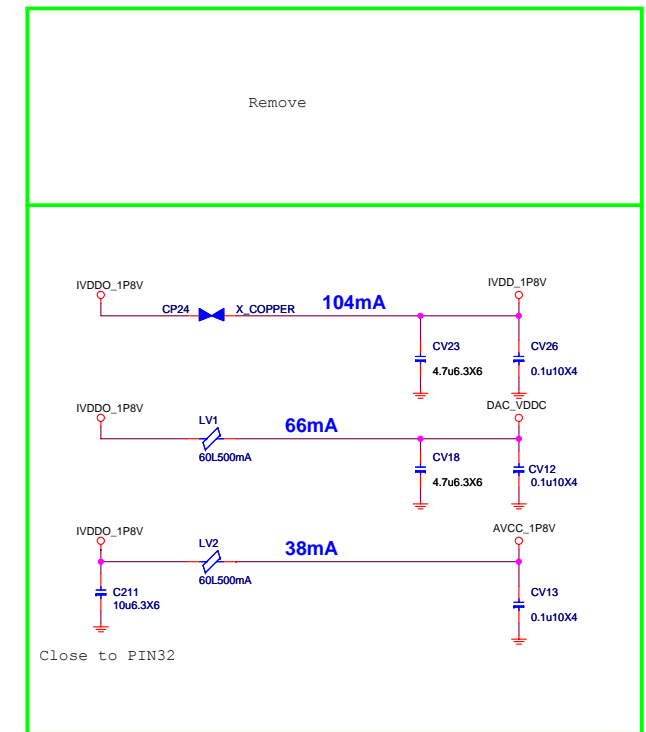
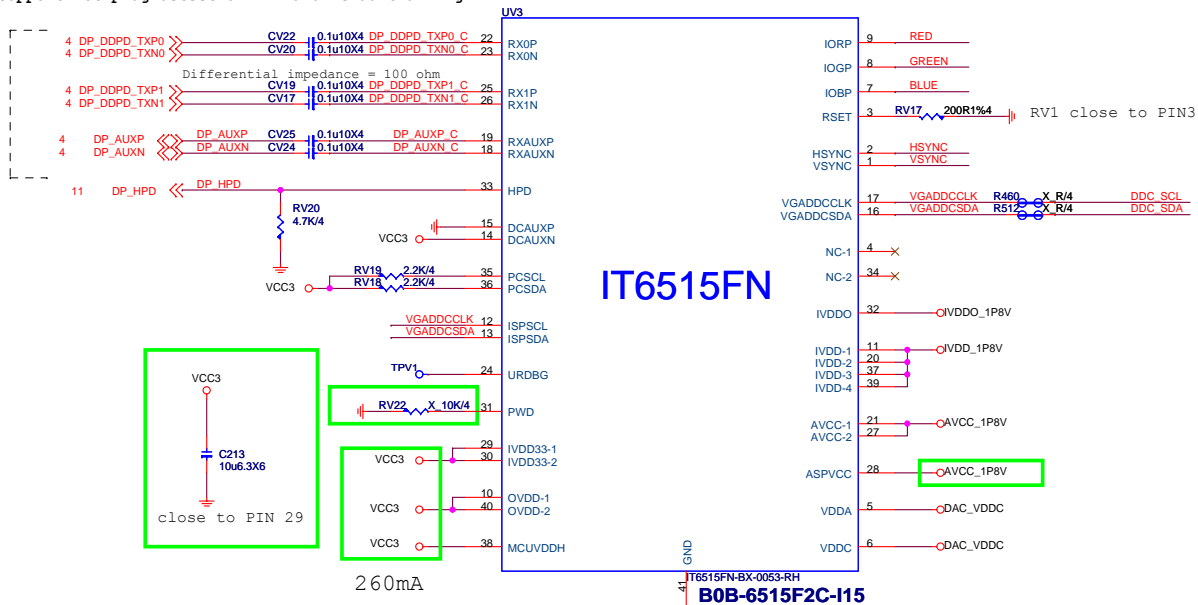
EMI cap.



	MICRO-STAR INT'L CO.,LTD		
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Note:

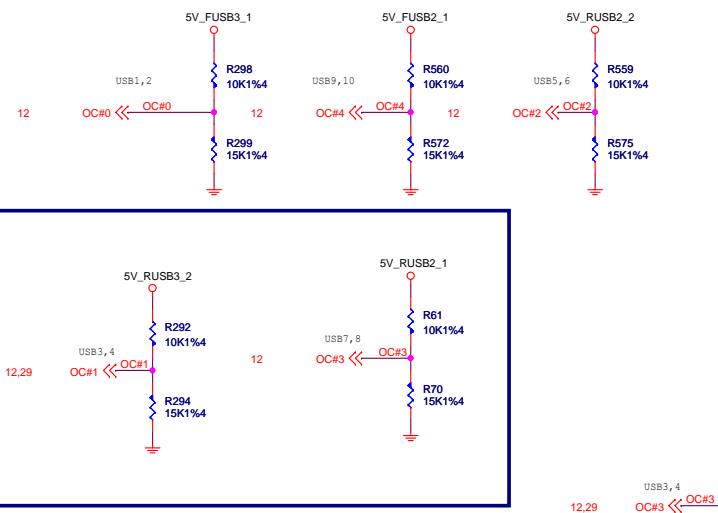
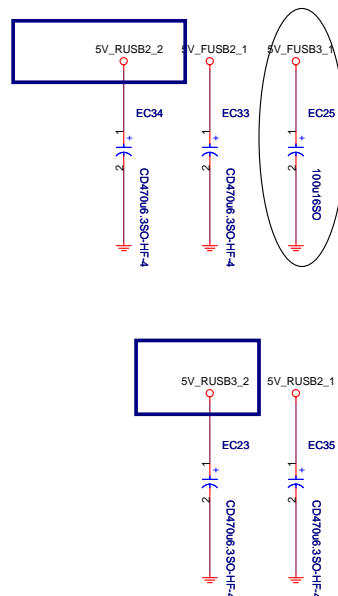
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



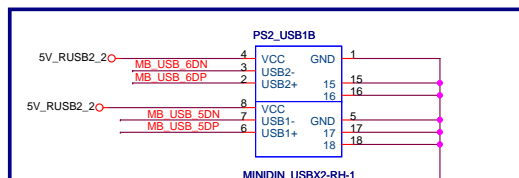
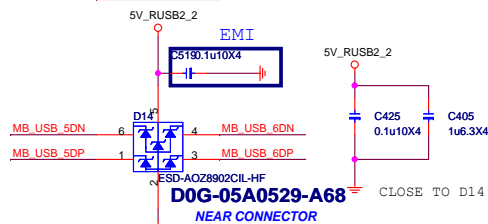
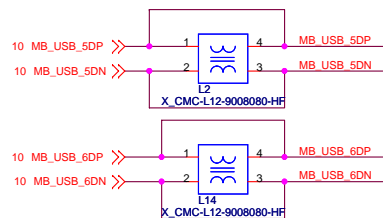
D0G-05A0519-A68

D0G-05A0519-A68

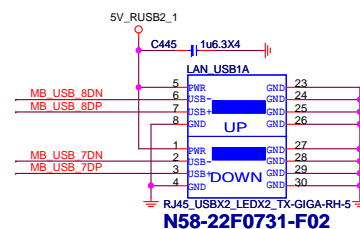
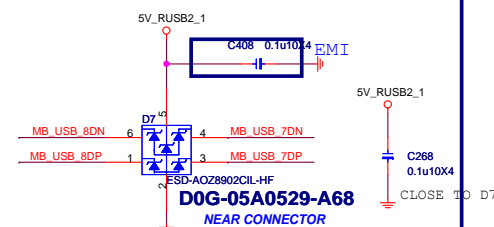
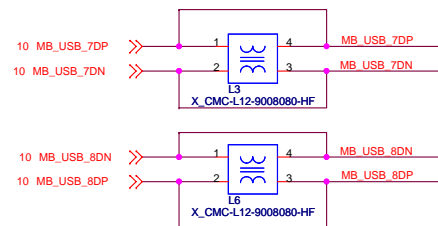
MICRO-STAR INT'L CO.,LTD		
MS-7A82		
Size	Document Description	Rev
Custom	VGA - ITE6S15	1.0
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FRONT USB PORT 5,6

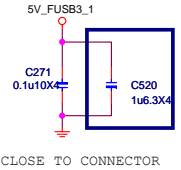
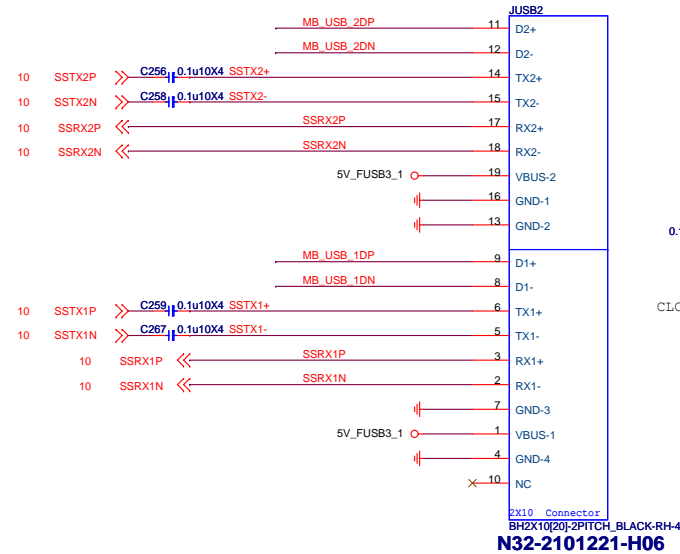
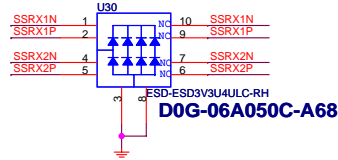
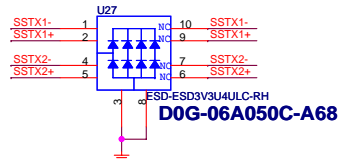
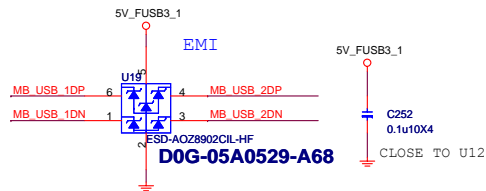
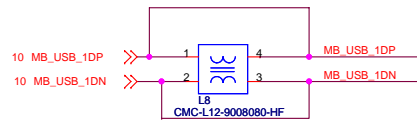
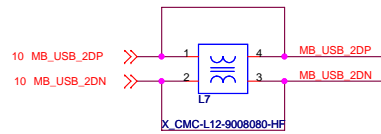


REAR USB PORT 7,8 (With LAN)

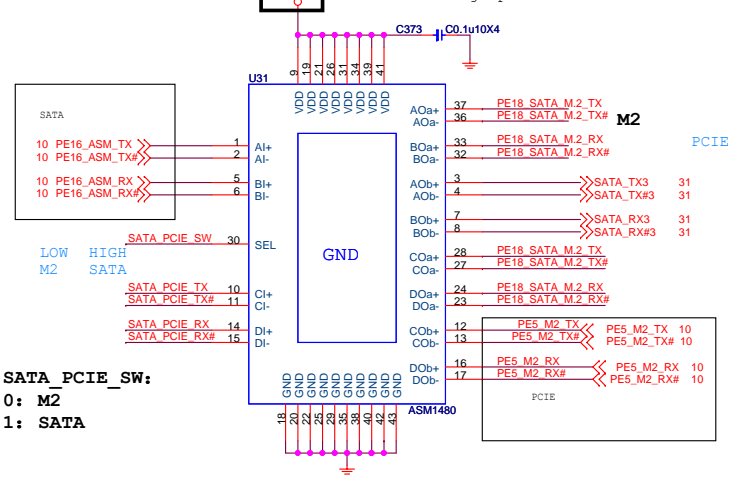


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2015.07.02 Change power source



SATA_PCIE_SW:
0: M2
1: SATA

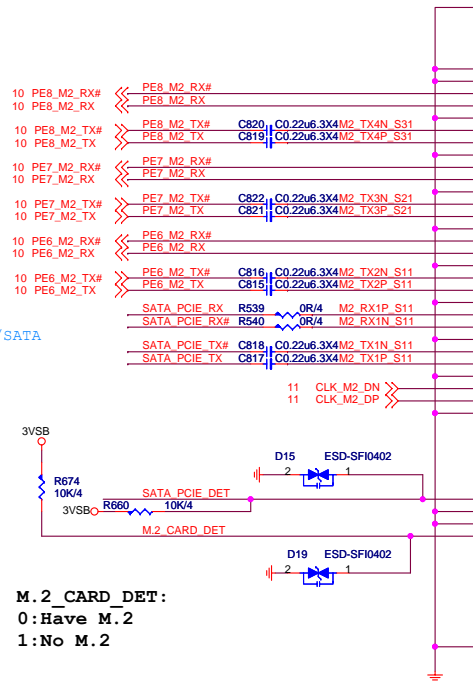
Truth Table

SEL	L	H
Function	IN+ to outa+	IN+ to outb+
Function	IN+ to outa+	IN+ to outb+

2015.07.02
Remove PU to M2_VCC3

SATA_PCIE_DET:
0: SATA
1: PCIE

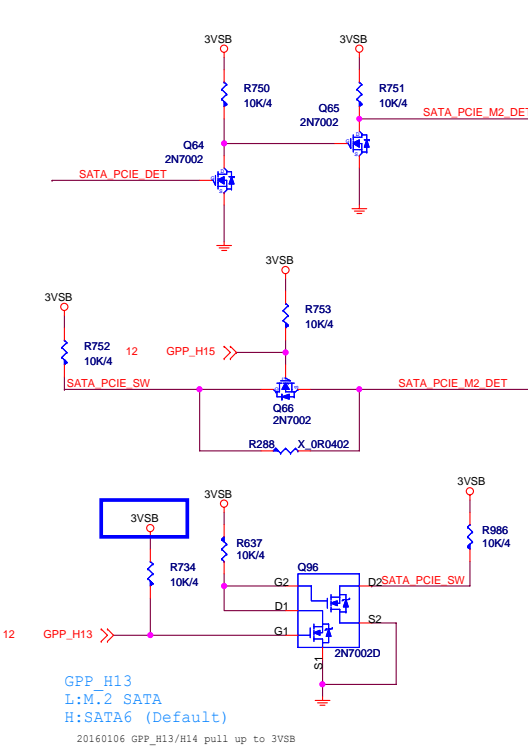
M.2_CARD_DET:
0: Have M.2
1: No M.2



KEY M

BIOS_MODE

M2_2_GPP5	M2_2_GPP7	Mode
0	0	M2-SATA
1	0	M2-PCIE
GPI	1	AUTO



GPP_H13
L:M.2 SATA
H:SATA6 (Default)
20160106 GPP_H13/H14 pull up to 3VSB

BIOS_MODE

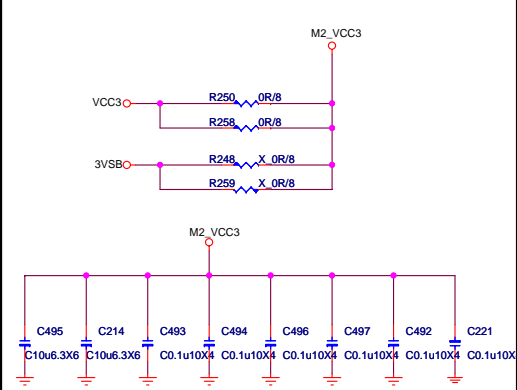
GPP_H13	GPP_H14	GPP_H15	Mode
GPI	GPI	GPI	AUTO
1	1	0	M.2_PCIE
0	0	0	M.2_SATA

HW_MODE

M.2_CARD_DET	SATA_PCIE_DET	M2_PCIE_DET	M.2	SATA6	PCIE_X4
None (1)	None (1)	None (0)	NA	1	1
Present (0)	SATA (0)	Present (0)	SATA	NA	1
Present (0)	PCIE (1)	Present (1)	PCIE	1	NA

SATA6GP
for chipset that main power,if pull up to VSB maybe will leakage power
if sampled value = 1, select SATA; if sampled value = 0, select PCIE

2.5A



H1 <HP-BOM> H2 <HP-BOM> H3 <HP-BOM>

E2B-7924010-RH E2B-7924010-RH E2B-7924010-RH

Footprint: H_R240D173_BR189_PT

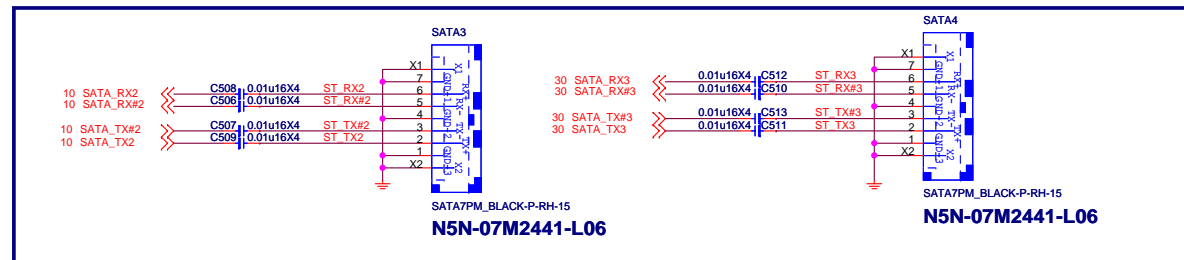
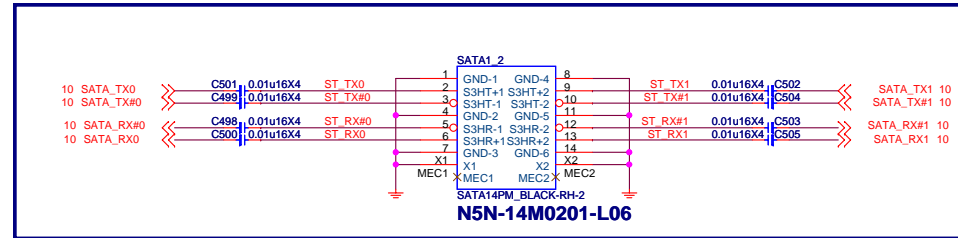
For 22110

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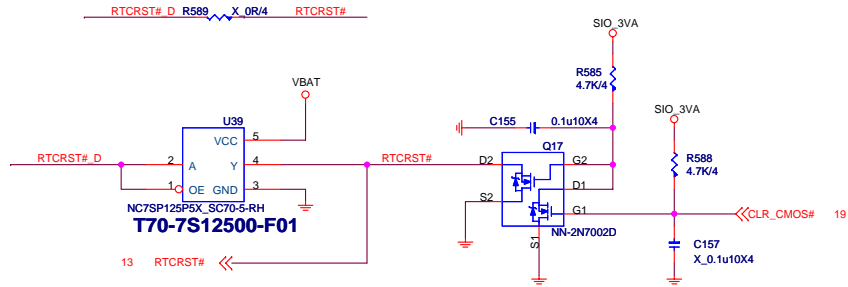
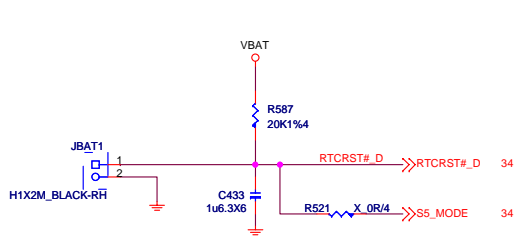
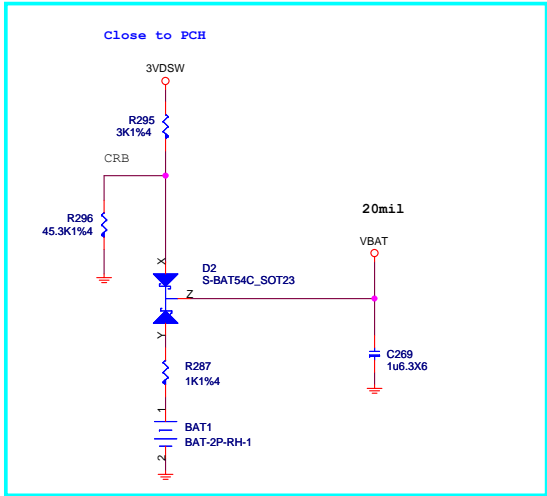
MS-7A82

Size Custom Document Description Rear USB3 & Front Connector Rev 1.0

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CUT_VBAT G3 Status



tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R589	U39	R587	C433
USE U39				
Auto CLR_CMOS	X	O	O	O
NOT USE U39				
Auto CLR_CMOS	O	X	X	X

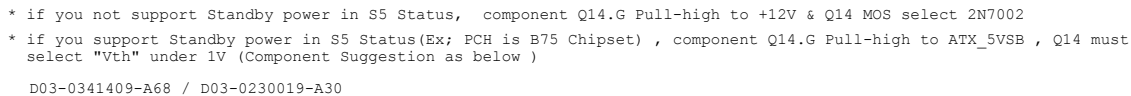


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Size	Document Description	Rev
Custom	CUT_VABT circuit	1.0
Date: Wednesday, June 22, 2016		Sheet 32 of 51

1. DPWROK と RSMRST#N 癖, T-PWROK 珍癖 ME code 積欄
2. 祚诀 符 VCC3 癖虫, SIO x PWROK い RSMRST#
3. 材 Ω 策 SLP S3# T-HI, / RSMRST# い ㄣ

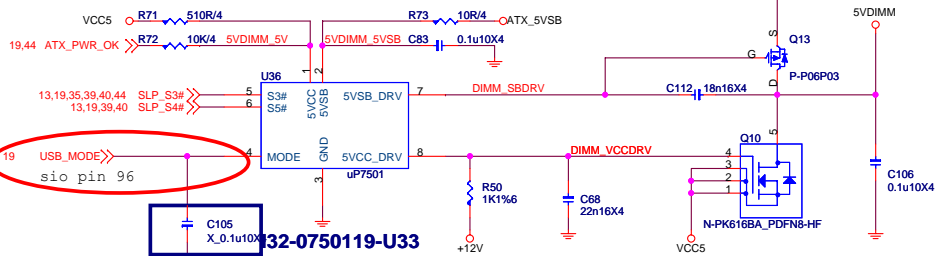


5VDIMM FOR DDR & USB
DDR:7.9A USB:6.6A

DDR: 7.9A USB: 6.6A

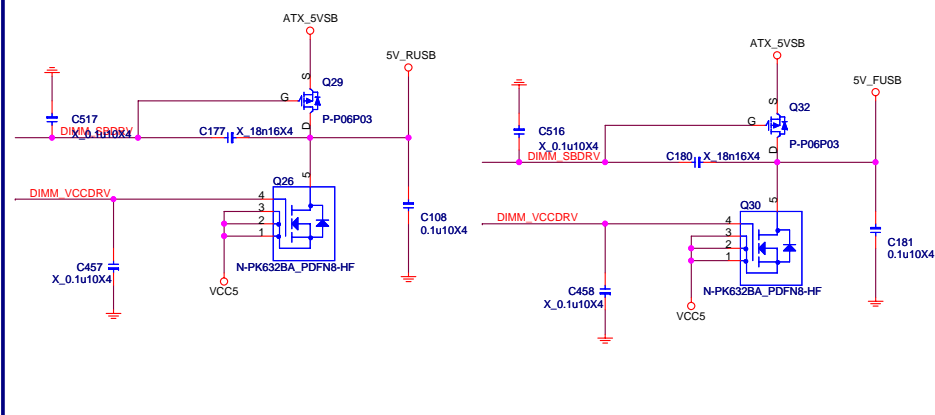
D03-06P0319-N03

14.5A



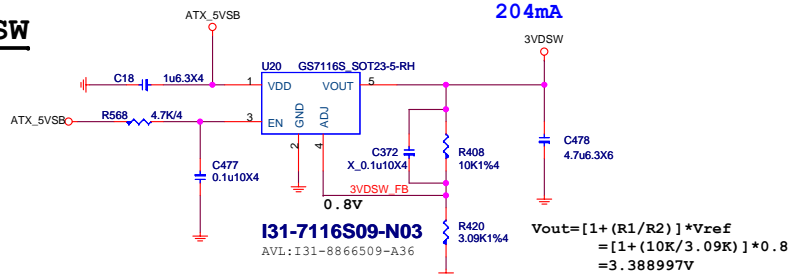
32-0750119-U33

D03-616BA0C-N03



3VDSW

204mA



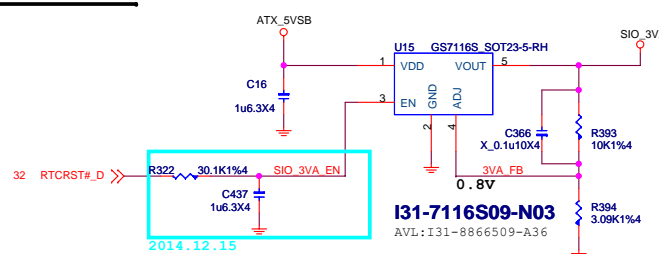
I31-7116S09-N03

AVL:I31-8866509-A36

$$\begin{aligned} V_{out} &= [1 + (R_1/R_2)] * V_{ref} \\ &= [1 + (10K/3.09K)] * 0.8 \\ &= 3.388997V \end{aligned}$$

SIO_3VA

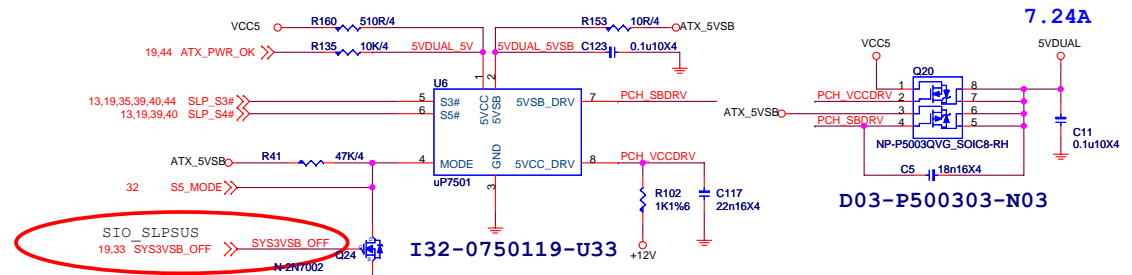
20mA



I31-7116S09-N03

AVL:I31-8866509-A36

5VDUAL FOR PCH_1VSB



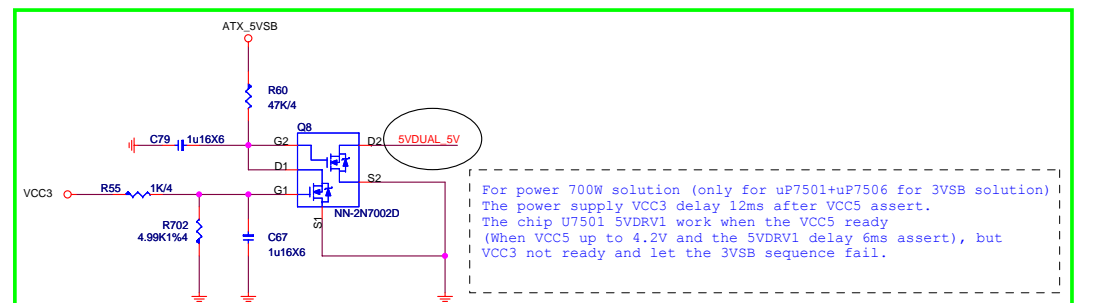
D03-P500303-N03

I32-0750119-U

```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

```
SYS3VSB_OFF (DSW POWER CONTROL)
default is set to 1 to cut off the standby power
DSW S5 (HIGH): USB no power
S5 (LOW): USB have power
```

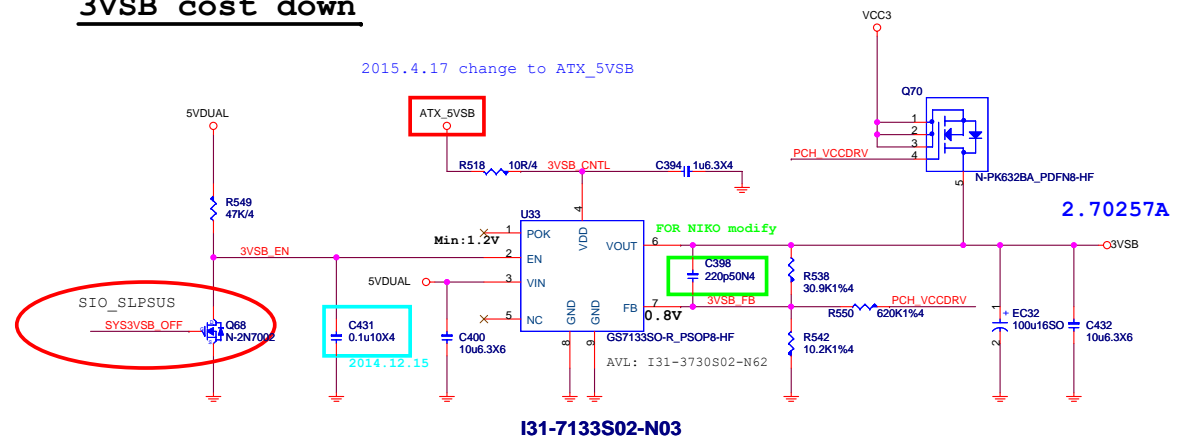
S5#	S3#	MODE	5VDIMM	Remark
1	1	X	VCC5	S0
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5



```
| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
| The power supply VCC3 delay 12ms after VCC5 assert.
| The chip U7501 5VDRV1 work when the VCC5 ready
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
| VCC3 not ready and let the 3VSB sequence fail.
```

3VSB cost down

2015.4.17 change to ATX_5VSB



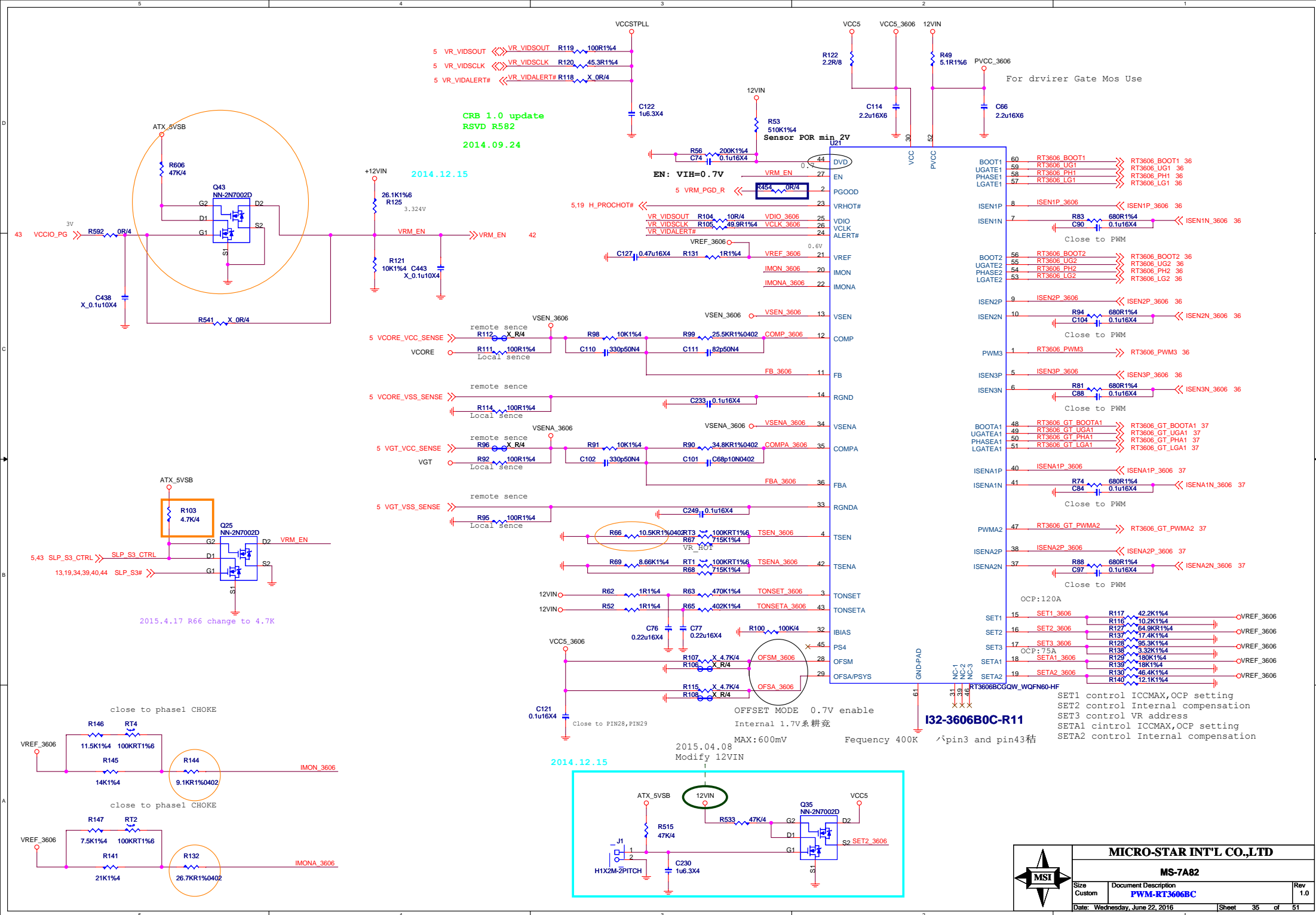
I31-7133S02-N03

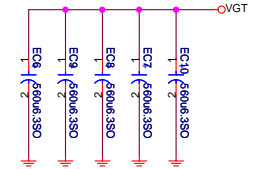
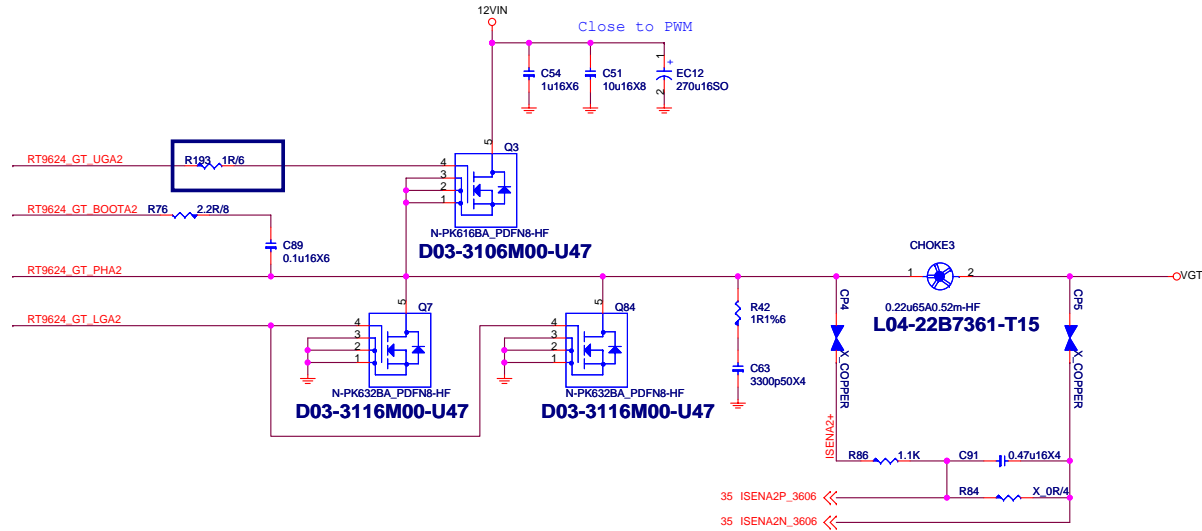
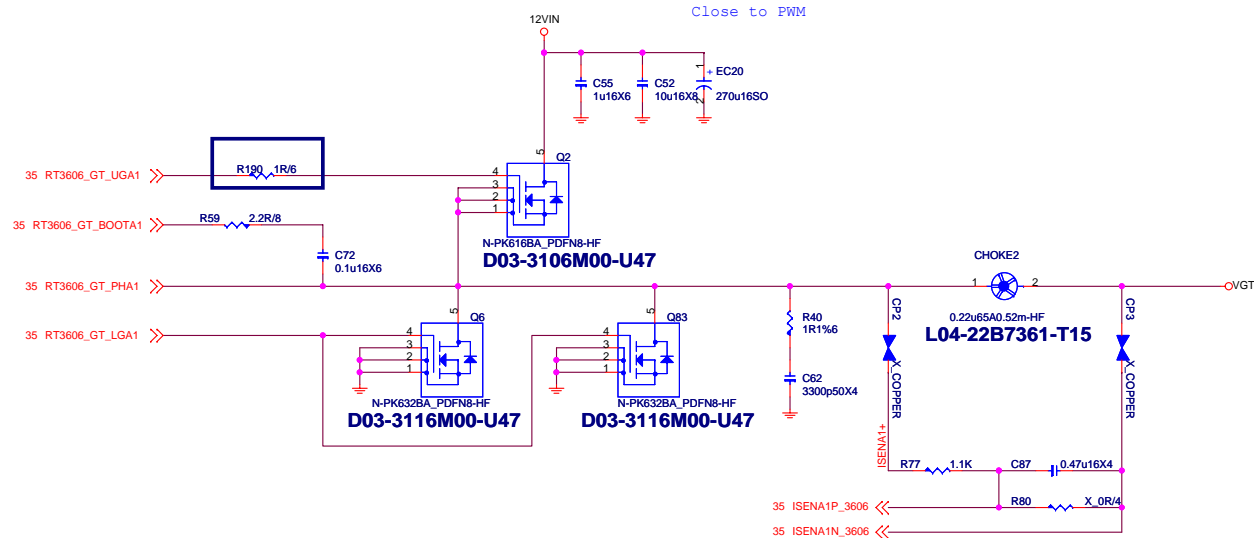
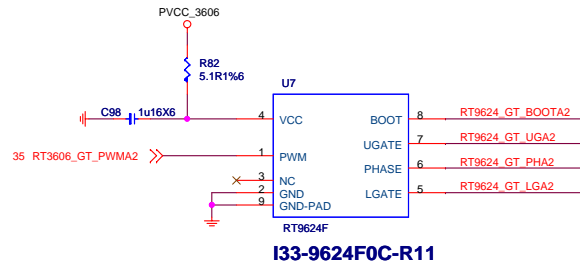
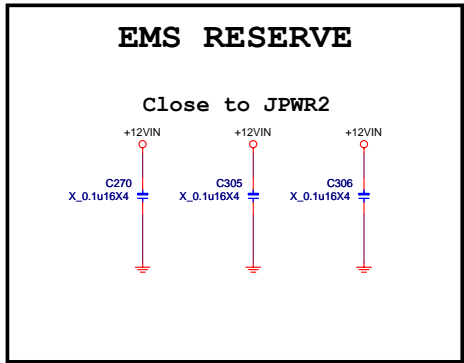
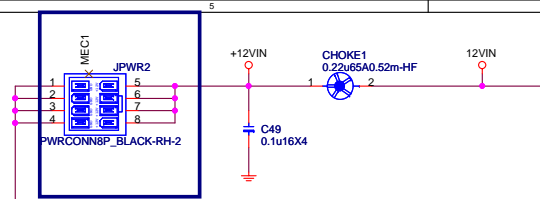


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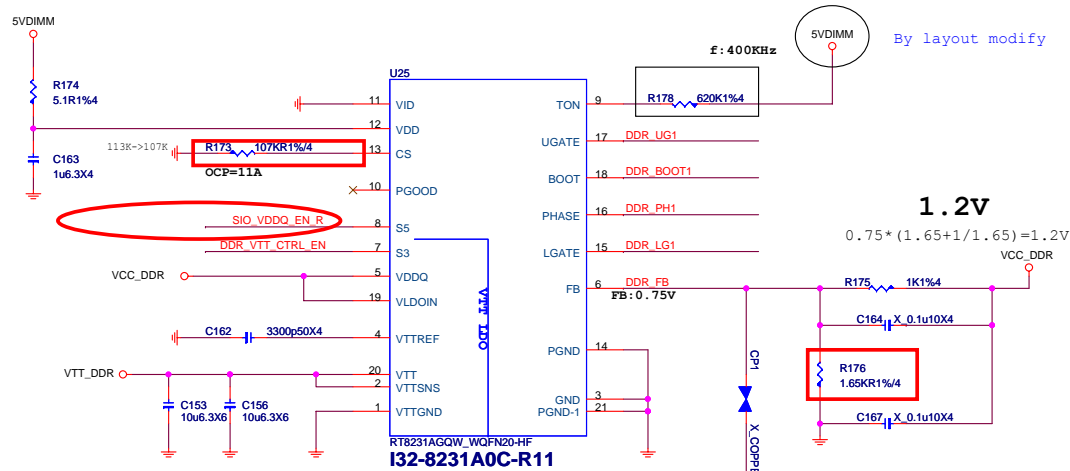
Size Custom	Document Description ACPI CONTROLLER	Rev 1.0
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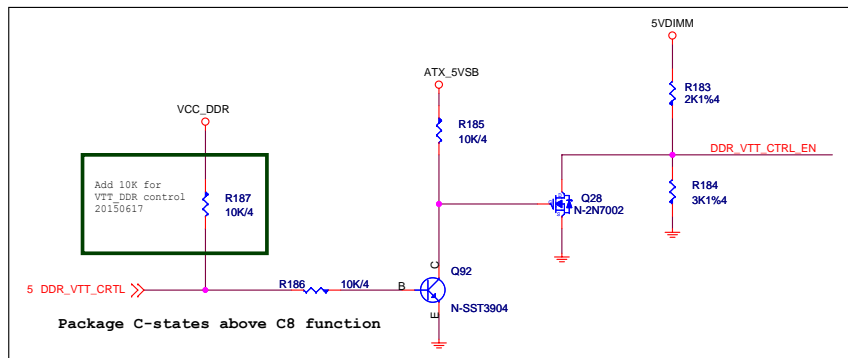
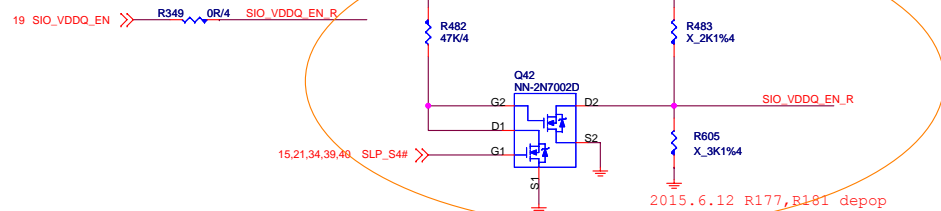


2.8A FOR CPU
4.8A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

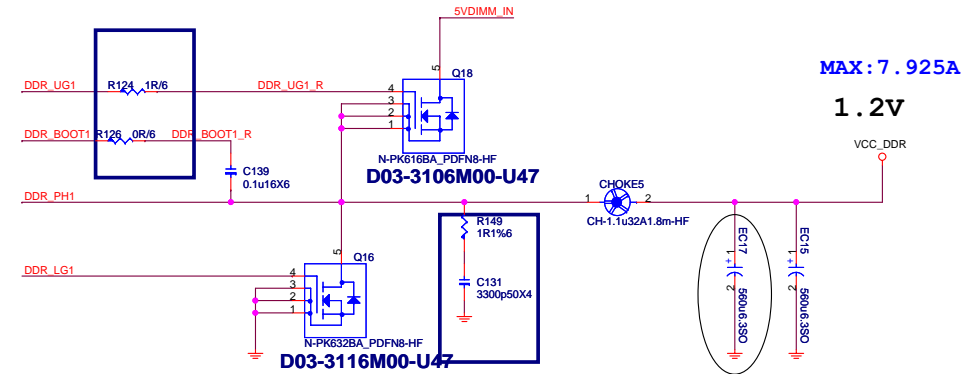
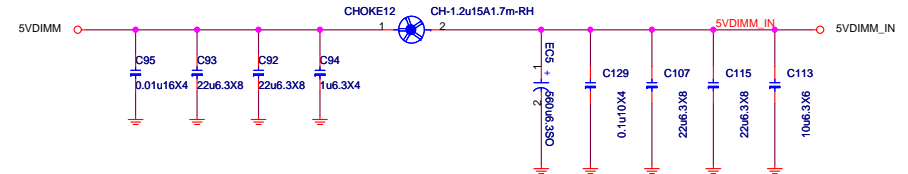
$$\text{Current limit} = 95.3\text{K}(R173) * 5\mu\text{A}/10/4\text{mohm} = 11.91\text{A}$$



2014.12.17 update
From SIO pin 87

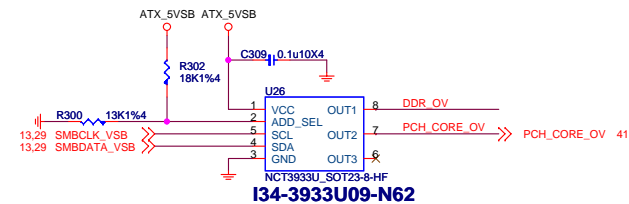


$$\begin{aligned} I_{rms} &= I_{out} * \text{SQRT}((V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))) \\ &= 9.357 * 0.44 \\ &= 4.154\text{A} \end{aligned}$$



UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K

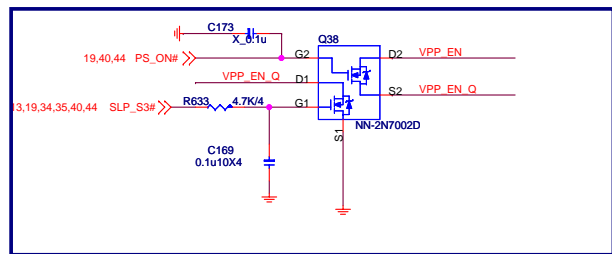
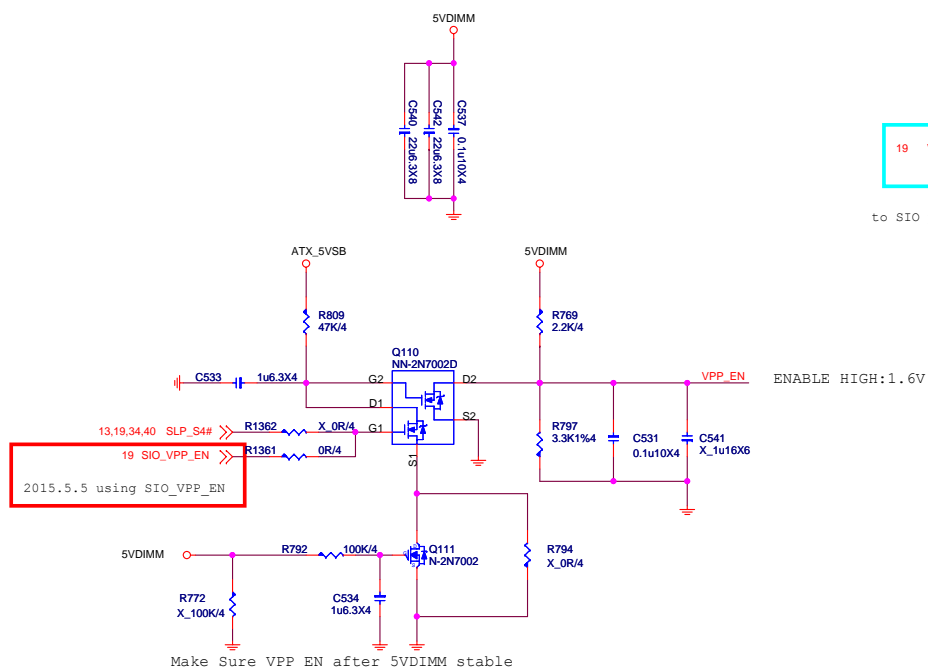


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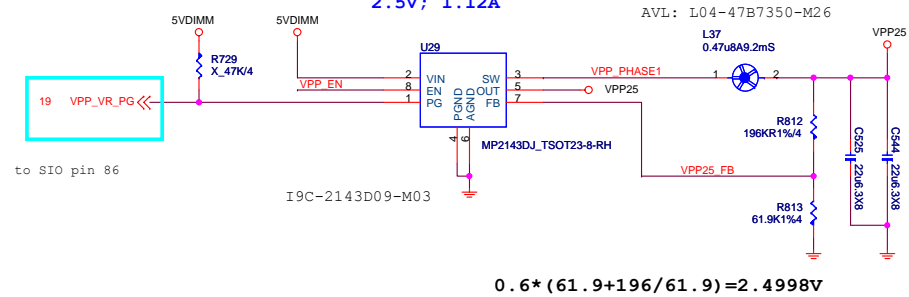
MS-7A82

Size Custom	Document Description DDR-RT8231AGQW	Rev 1.0
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2DIMM :1.12A FOR DDR VPP2.5V



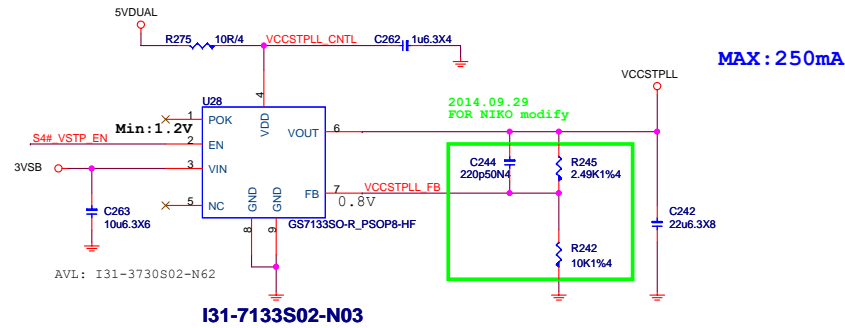
VPP25 Power 2.5V; 1.12A



VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

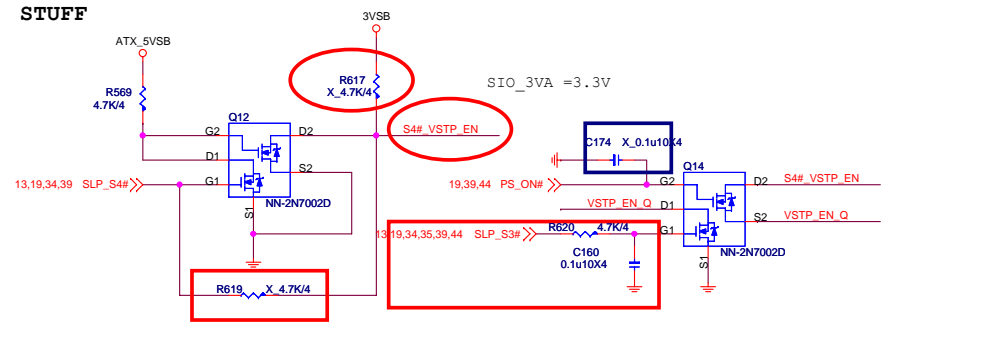


VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

20151623 Fix G3->S5 PWR auto enable

STUFF



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Size	Document Description	Rev
Custom	CPU PWR_ST/PLL	1.0
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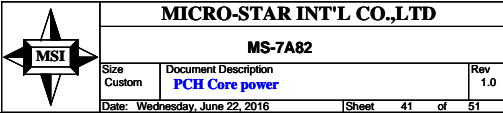
1.0V; 7.24A

```
Rocset = 1.5 * Imax * Rdson(low) / Iocset
        = 1.5 * 7.24 * 4.6mohm / 10uA
        = 4.9956K
```

Rdson (low) 4.5V

D03-4C05N03-O05	:	5 mohm
D03-632BA0C-N03	:	4.6mohm
D03-3056M00-U47	:	6.2mohm

Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

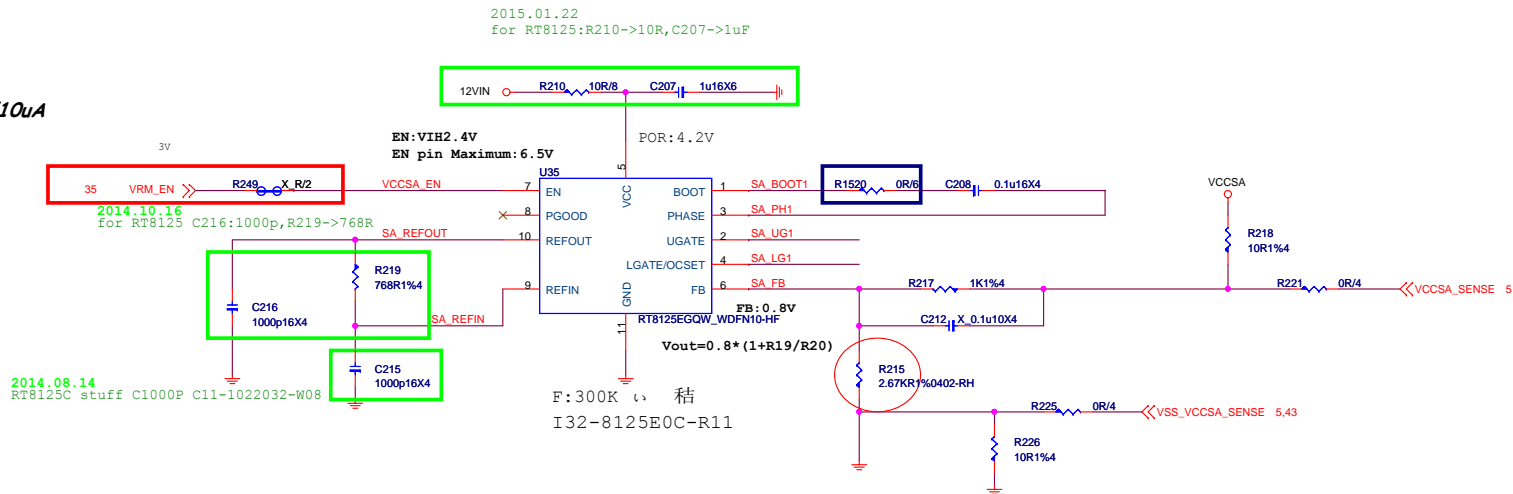


SA Power:1.05V,11.1A

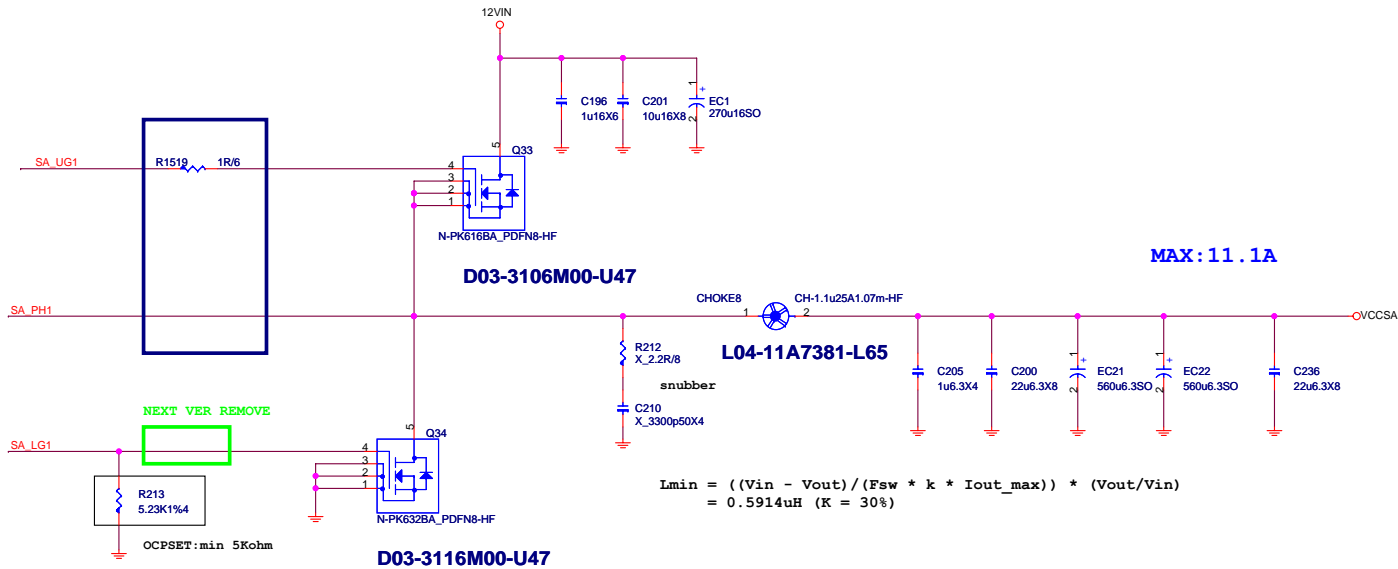
OCP = 11.1A*1.4=15.54A
Rocs(R15)=OCP*Rdson(Low side)3.3mohm/10uA
=15.54*(3.3)mohm/10uA
=5.2836Kohm

Rocs: 5.2836K, OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson (low) 10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

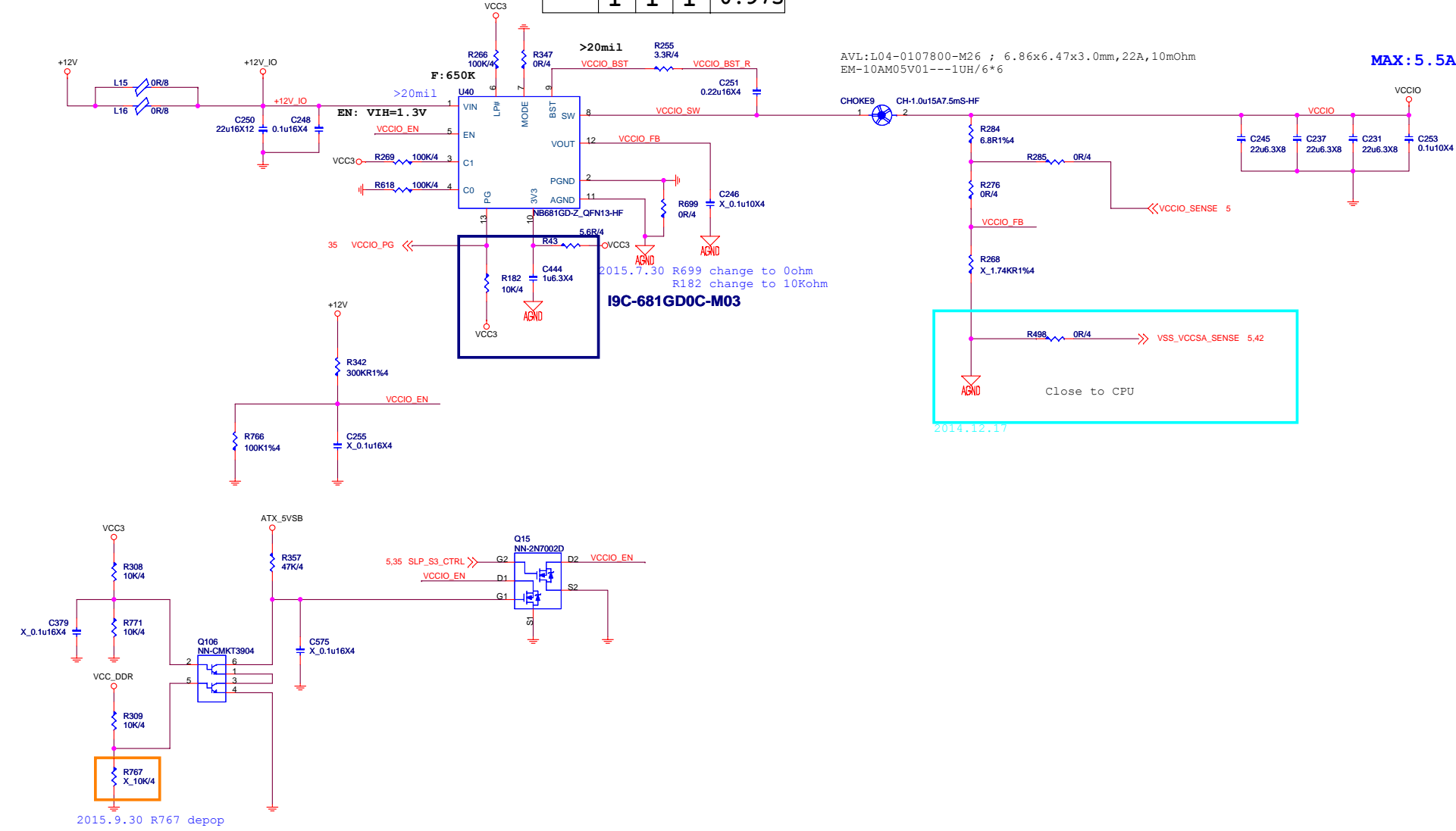


$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$
$$= 11.1 * 0.2825$$
$$= 3.13575A$$



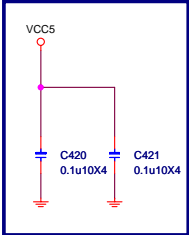
VCCIO
0.95V; 5.5A
IMAX 6A
ILIMIT=8.5~9A

	LP#	C1	C0	VOU _T (V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



```
19,39,40 PS_ON#>>>
```

remove power fault



Pin configuration diagram for the I36-7550PMA8-U33 component. The component is a square package with pins 1 through 8. Pin 1 is labeled 'S3#' and 'OC#'. Pin 2 is labeled 'VOUT1'. Pin 3 is labeled 'VOUT2'. Pin 4 is labeled 'EN'. Pin 5 is labeled '5VCC'. Pin 6 is labeled '5VSSB'. Pin 7 is labeled 'GND'. Pin 8 is labeled 'GND'. The component is identified as 'UP7550PMA8_SOT23-8-HF' and 'I36-7550PMA8-U33'. The diagram shows connections for '13,19,34,35,39,40' to 'SLP_S3#' and '19' to 'PS2_MODE'. A capacitor 'C3 22uF 3x8' is connected to pin 7.

[illegible]

The schematic diagram shows the JFP1 module (H2X5[10]M_BLACK-RH) with the following connections:

- VCC5**: Connected to pin 1 (HDD+) via resistor R570 (330R/6).
- HDD+**: Connected to pin 1 (HDD+).
- HDD-**: Connected to pin 3 (HDD-).
- RESET-**: Connected to pin 5 (RESET-).
- NC**: Connected to pin 7 (NC).
- PLED**: Connected to pin 2 (PLED).
- SLED**: Connected to pin 4 (SLED).
- PSIN#**: Connected to pin 6 (PSIN#) via resistor R557 (100R).
- PWSW-**: Connected to pin 8 (PWSW-).
- PWR LED**: Connected to pin 2 (PLED).
- SUS LED**: Connected to pin 4 (SLED).
- PSIN# R**: Connected to pin 6 (PSIN#) via resistor R557 (100R).
- PWRBTIN**: Connected to pin 6 (PSIN#) via resistor R557 (100R).
- SIO_3VA**: Connected to pin 6 (PSIN#) via resistor R573 (10K/4).
- FP_RST#**: Connected to pin 13 (FP_RST#) via resistor R574 (33R/4).
- FP_RST# R**: Connected to pin 13 (FP_RST#) via resistor R574 (33R/4).
- C426**: Connected to pin 1 (HDD+) via capacitor C426 (0.1u10X4).
- C427**: Connected to pin 3 (HDD-) via capacitor C427 (0.1u10X4).
- C424**: Connected to pin 5 (RESET-) via capacitor C424 (0.1u10X4).
- C423**: Connected to pin 6 (PSIN#) via capacitor C423 (0.1u10X4).

R=390 Ohm
 $I=(5-0.2)/R=0.0123\text{ A}$
 $W=0.0123\text{ A} \times 5\text{V}=0.0615\text{W}$ (鎊環零)
 $R=1/16\text{W}=0.062\text{W}$

30 M2_DAS

R614 5.1K1%4

NN-CMKT3904

2 6 1 3 4 5

Q97

M2_VCC3

R591 5.1K1%4

HDD_LED

The schematic diagram illustrates the PS2 to USB interface circuit. The PS2_PWR input is connected to a network of resistors (R20, R25, R45, R18, R28) and a capacitor (C1). The PS2_USB1A connector is shown with pins for VCC, DT, CK, and MS. A callout box provides the pin connections for the PS2_USB1A connector:

PS2_USB1A	Pin	Signal
VCC	10	12
DT	11	13
CK	13	14
MS	14	15

The circuit also includes a 74V04 hex inverter (U17) and a capacitor (C53) connected to the PS2_PWR input. The PS2_PWR input is connected to the PS2_USB1A connector via a network of resistors (R20, R25, R45, R18, R28) and a capacitor (C1). The PS2_USB1A connector is shown with pins for VCC, DT, CK, and MS. A callout box provides the pin connections for the PS2_USB1A connector:

PS2_USB1A	Pin	Signal
VCC	10	12
DT	11	13
CK	13	14
MS	14	15

Diagram illustrating the connection of the H2X7(10)M-2PITCH_BLACK-RH module to the LPC1114 microcontroller.

Microcontroller Pins (LPC1114):

- 11 TPM_CLK
- 19 PLTRST_BU1#, TPM
- 13,19 LPC_ADO
- 13,19 LPC_AD1
- 13,19 LPC_AD2
- 13,19 LPC_AD3
- 13,19 LPC_FRAME#

Module Pins (H2X7(10)M-2PITCH_BLACK-RH):

- 1 JTPM1
- 2
- 4
- 6
- 8
- 9
- 11
- 12
- 13
- 14

Connections:

- 3VSB connects to JTPM1 pin 1.
- VCC3 connects to JTPM1 pin 2.
- VCC5 connects to JTPM1 pin 4.
- TPM_CLK (11) connects to JTPM1 pin 1.
- PLTRST_BU1# (19) connects to JTPM1 pin 2.
- LPC_ADO (13,19) connects to JTPM1 pin 4.
- LPC_AD1 (13,19) connects to JTPM1 pin 6.
- LPC_AD2 (13,19) connects to JTPM1 pin 8.
- LPC_AD3 (13,19) connects to JTPM1 pin 10.
- LPC_FRAME# (13,19) connects to JTPM1 pin 12.

Module Components:

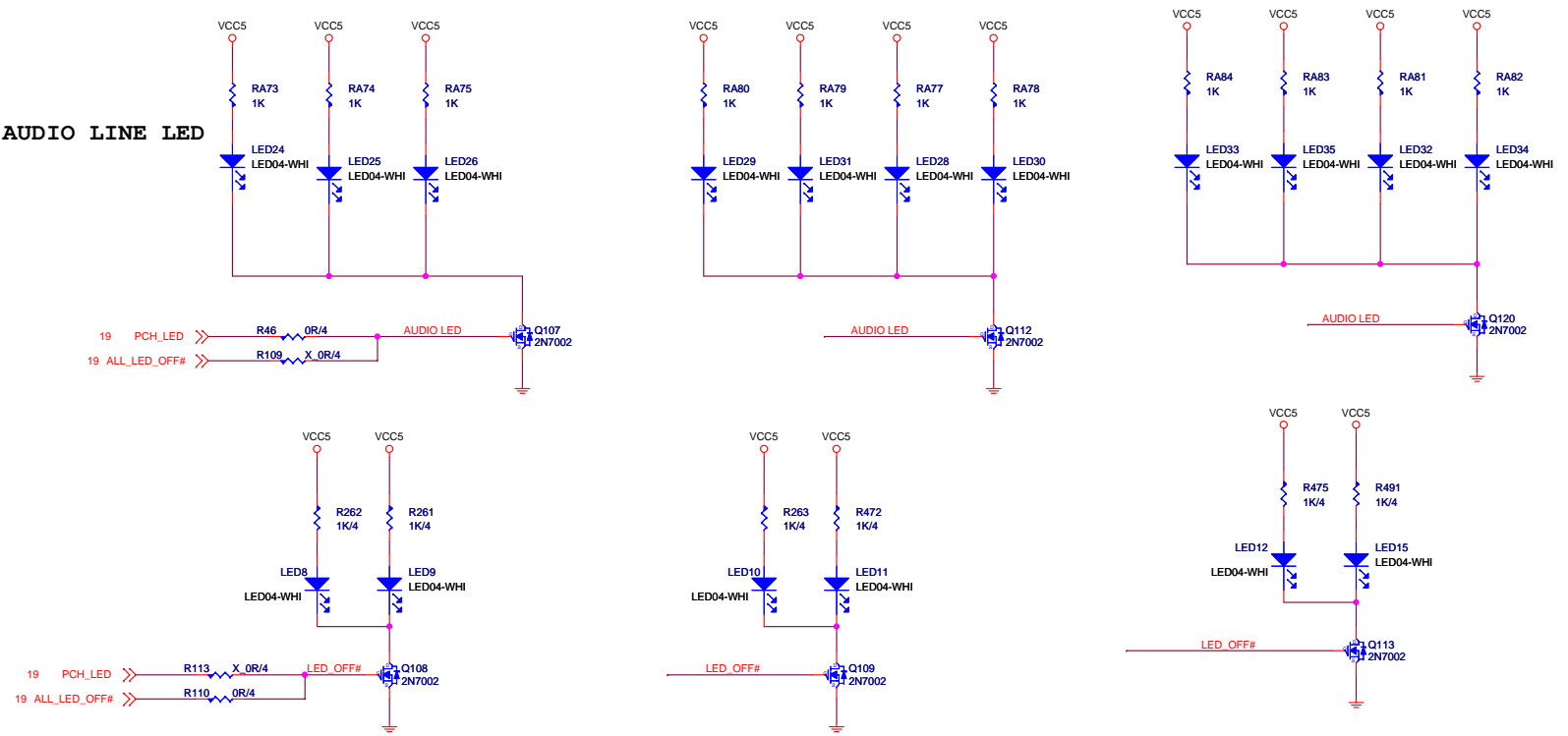
- C344 (0.1uF)
- C343 (0.1uF)
- C342 (0.1uF)

Module Label: H2X7(10)M-2PITCH_BLACK-RH



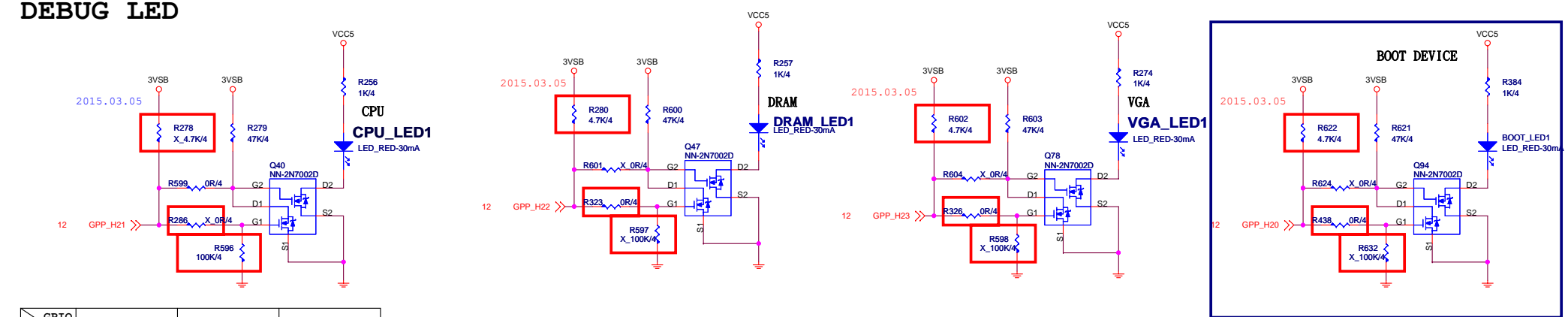
Size Custom	Document Description ATX F_Panel/TPM/MSI_LED	Rev 1.0
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AUDIO LINE LED



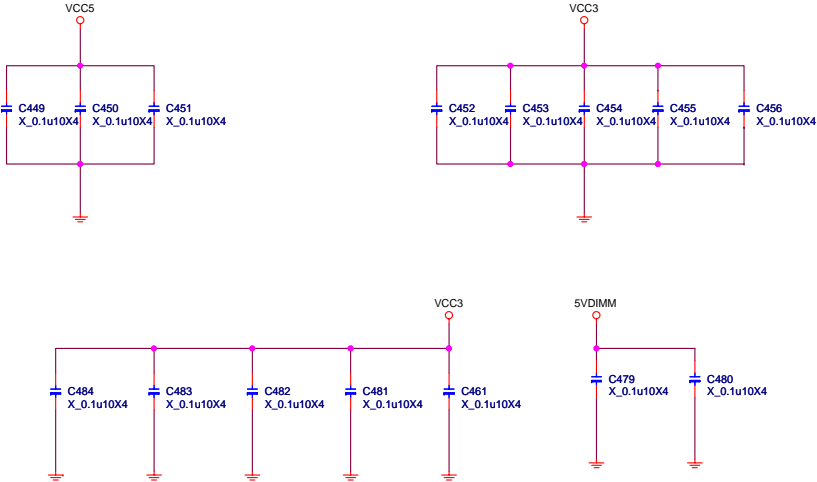
DEBUG LED 璦T璦 ン, 尤いR278, R599, R280, R601, R602, R604 い ン, 尤緇 璦 ン

DEBUG LED



GPIO LED	GPP_H21	GPP_H21	GPP_H21
獺	GPI (default LOW)	GPI (default LOW)	GPI (default LOW)
防	HIGH	HIGH	HIGH

EMI CAP





BAT-BCR2032P-RH



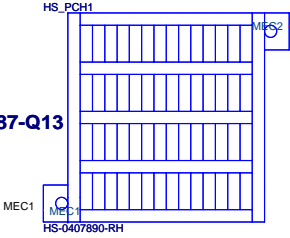
CPU_H1



H110M



H110M



HS-0407890-RH



7A82-QA

PD0-07A8210-G37

PK0-07A4810-G37 弘θ-襲, 23, 脚 吹邻紅 (MSIS)
PK0-07A4810-E48, 襲地, 23, 脚 吹邻紅 (MSIS)



X_REF5



HDMI LABEL



Y02-MU00170-CFO



Y02-MA00101-SSE

Nahimic Label

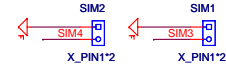
E21-7869020-F02

G51-M1SPJ88-Q13

G51-M1SPJ87-Q13

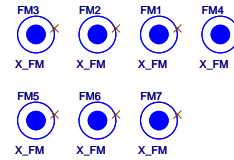
G51-M1SPXXA-A09

Simulation

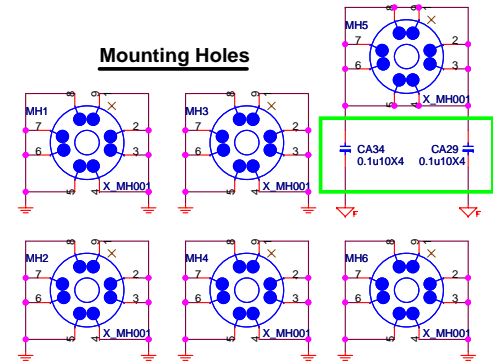


VCC_DDR		VCC_DDR
VTT_DDR		VTT_DDR
5VDIMM		5VDIMM
5VDUAL		5VDUAL
3VSB		3VSB
VBAT		VBAT
3VDSW		3VDSW
PCH_1VSB		PCH_1VSB
VCORE		VCORE
VGTT		VGTT
VCCSA		VCCSA
VCCSTPLL		VCCSTPLL
VCCIO		VCCIO

Optical Fiducial Marks-120



Mounting Holes



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MS-7A82

Size	Document Description	Rev
Custom	Manual Parts	1.0
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